Instruction Manual

Tektronix

DAS 92DM72A
Am29000 & Am29050
Microcontroller Support

070-8477-00

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

Please check for change information at the rear of this manual.

First Printing: November 1991
Revised Printing: March 1993
Online Document: April 1997

Instrument Serial Numbers

Each instrument manufactured by Tektronix has a serial number on a panel insert or tag, or stamped on the chassis. The first letter in the serial number designates the country of manufacture. The last five digits of the serial number are assigned sequentially and are unique to each instrument. Those manufactured in the United States have six unique digits. The country of manufacture is identified as follows:

B010000	Tektronix, Inc., Beaverton, Oregon, USA
E200000	Tektronix United Kingdom, Ltd., London
J300000	Sony/Tektronix, Japan
H700000	Tektronix Holland, NV, Heerenveen, The Netherlands

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Tektronix, Inc., P.O. Box 500, Beaverton, OR 97077

Printed in U.S.A.

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Preface: GUIDE TO DAS 9200 DOCUMENTATION

The Digital Analysis System (DAS) 9200 documentation package provides the information necessary to install, operate, maintain, and service the DAS 9200. The DAS 9200 documentation consists of the following:

- a series of microprocessor-specific **microprocessor support instructions** that describe the various microprocessor support packages
- a **system user's manual** that includes a beginning user's orientation, a discussion of DAS 9200 system-level operation, and reference information such as installation procedures, specifications, error messages, and a complete system glossary
- a series of **module user's manuals** that describe each of the DAS 9200 acquisition, pattern generation, and optional I/O modules
- an **on-line documentation** package that includes "context-sensitive" technical notes
- a **programmatic command language user's manual** that describes the set of programmatic commands available for remotely controlling the DAS 9200
- a series of **application software user's manuals** that describe the various application software packages
- a **technician's reference manual** that helps a qualified technician isolate DAS 9200 problems to the individual module level and determine corrective action (including on-site removal and replacement of modules)
- a **verification and adjustment procedures manual** that allows a qualified technician to make necessary adjustments and verify specifications of the mainframe and modules
- a series of **workbooks** that teach concepts about DAS 9200 acquisition modules and pattern generation modules

GENERAL SAFETY SUMMARY

The general safety information in this summary is for operating and servicing personnel. Specific warnings and cautions can be found throughout the manual where they apply, and may not appear in this summary.

TERMS IN THIS MANUAL

CAUTION

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

TERMS AS MARKED ON EQUIPMENT

CAUTION indicates a hazard to property, including the equipment itself, and could cause minor personal injury.

WARNING indicates solely a personal injury hazard not immediately accessible as you read the marking.

DANGER indicates a personal injury hazard immediately accessible as you read the marking.

SYMBOLS AS MARKED ON EQUIPMENT

DANGER—High voltage.

Protective ground (earth) terminal.

ATTENTION—REFER TO MANUAL.

GROUNDING THE PRODUCT

This product is intended to operate from a power source that does not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground.

WARNING: This product is grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle. A protective-ground connection by way of the grounding conductor in the power cord is essential for safe operation. (I.E.C. Safety Class I)

DANGER ARISING FROM LOSS OF GROUND

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulated) can render an electric shock.

POWER DISCONNECT

The main power disconnect is by means of the power cord or, if provided, an ac power switch.

USE THE PROPER POWER CORD

Use only the power cord and connector specified for your product. Use only a power cord that is in good condition. CSA Certification includes the equipment and power cords appropriate for use on the North America power network. All other power cords supplied are approved for the country of use.

USE THE PROPER FUSE

To avoid fire hazard use only a fuse of the correct type, voltage rating, and current rating.

USE THE PROPER VOLTAGE SETTING

Make sure the line selector is in the proper position for the power source being used.

REMOVE LOOSE OBJECTS

During disassembly or installation procedures, screws or other small objects may fall to the bottom of the mainframe. To avoid shorting out the power supply, do not power-up the instrument until such objects have been removed.

USE CARE WITH COVERS REMOVED

To avoid personal injury, remove jewelry such as rings, watches, and other metallic objects before removing the cover. Do not touch exposed connections and components within the product while the power cord is connected.

REMOVE FROM OPERATION

If you have reason to believe that the instrument has suffered a component failure, do not operate the instrument until the cause of the failure has been determined and corrected.

DO NOT OPERATE IN EXPLOSIVE ATMOSPHERES

To avoid explosion, do not operate this product in an explosive atmosphere unless it has been specifically certified for such operation.

Section 1: OVERVIEW

The 92DM72A Microprocessor Support product disassembles data from systems based on the Advanced Micro Devices Am29000 or Am29050 microprocessor. The 92DM72A product runs on a DAS 9200 equipped with one or two 92A96 Data Acquisition Modules.

This product consists of software on a floppy disk, a probe adapter, and this manual. The software includes both setup files and a disassembler program.

Included in the software files are two demonstration reference memories. These files (called 29000_Demo and 29050_Demo) show disassembled data; they are automatically installed on the DAS 9200 when you install the disassembler software. All figures in Section 4 that show acquired data are taken from these demonstration reference memories. Directions for viewing the 29000_Demo and 29050_Demo files are in Section 3.

BASIC INFORMATION

To use this product, you need to have the following:

- this manual
- other DAS 9200 mainframe and data acquisition module user's manuals
- knowledge of your specific DAS 9200 configuration and its operation
- the *Am29000 32-Bit Streamlined Instruction Processor User's Manual* (Advanced Micro Devices, 1988), or the *Am29050 Streamlined Instruction Microprocessor Advance Information Manual* (1990) and the *Am29050 Microprocessor User's Manual* (1991)
- knowledge of your Am29000/050 system

DAS 9200 System Software Compatibility

The Am29000/050 Microprocessor Support is compatible with DAS 9200 System Software Release 2, Version 1.5 or greater. It is not compatible with previous system software versions.

About This Manual

The organization of this manual is based on the sequence of steps necessary to use the disassembler. If you are an experienced DAS 9200 user familiar with loading software and connecting microprocessor support probe adapters to a system under test, you can use the *Quick Start* section. The *Quick Start* section gives brief instructions on how to install the 92DM72A software, connect the DAS 9200 to your Am29000/050 system, and configure the probe adapter. You can then proceed to either Section 4 or 5 depending on whether you're using disassembly or performing hardware analysis.

If you are using DAS 9200 microprocessor support for the first time, you should read some sections sequentially. Read Sections 1, 3, and 4 if you are going to acquire and view disassembled data. Read Sections 1, 3, and 5 if you are going to acquire and view timing or state data for hardware analysis. Figure 1-1 shows how to proceed through this manual.

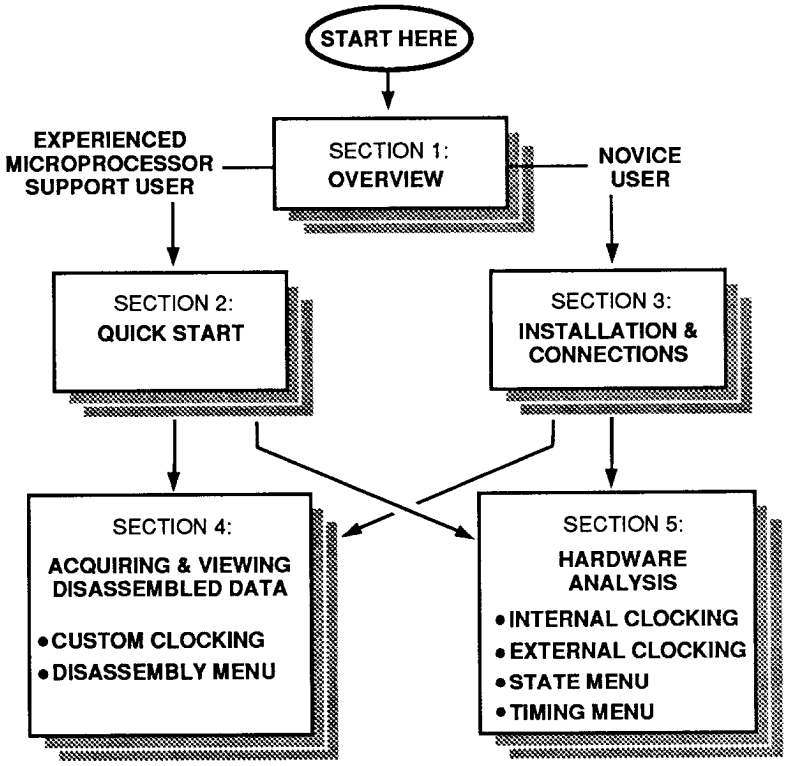

Figure 1-1. How to proceed through this manual.

In this manual, the following conventions are used:

- the terms disassembler and disassembler software are used interchangeably in reference to the 92DM72A software that disassembles the bus cycles into instruction mnemonics and cycle types
- the terms system under test and SUT are used interchangeably in reference to the microprocessor system under test
- references to the 92A96 Data Acquisition Module include all versions of that module unless otherwise noted
- the instruction bus for the Am29000/050 is called the code bus due to multimodule naming constraints in the DAS 9200
- a signal that is active low has an asterisk (*) before its name

Other Necessary Manuals

Before using these instructions, you should be familiar with the operation of a DAS 9200 with the data acquisition module you are using. For general instructions on the use of the DAS 9200 and a data acquisition module, refer to both the *DAS 9200 System User's Manual* and the data acquisition module user's manual.

Refer to Advanced Micro Device's *Am29000 32-Bit Streamlined Instruction Processor User's Manual* (1988) for information about the Am29000 microprocessor.

Refer to Advanced Micro Device's *Am29050 Streamlined Instruction Microprocessor Advance Information Manual* (1990) and the *Am29050 Microprocessor User's Manual* (1991) for information about the Am29050 microprocessor.

DAS 9200 Configuration

To use the Am29000/050 microprocessor support, your DAS 9200 must be equipped with one or two 92A96 Data Acquisition Modules with probe cables and standard probes.

The standard probe consists of four sets of one clock probe and three 8-channel probes each. The clock probe (a single channel) and each channel of the 8-channel probe has one signal connection and one ground connection. Leadsets and grabber tips are not required.

When operating with one module, you can only acquire data from either the code bus or the data bus. When operating with two modules, you can acquire data from both buses.

Figure 1-2 shows an overall view of the DAS 9200 connected to a system under test.

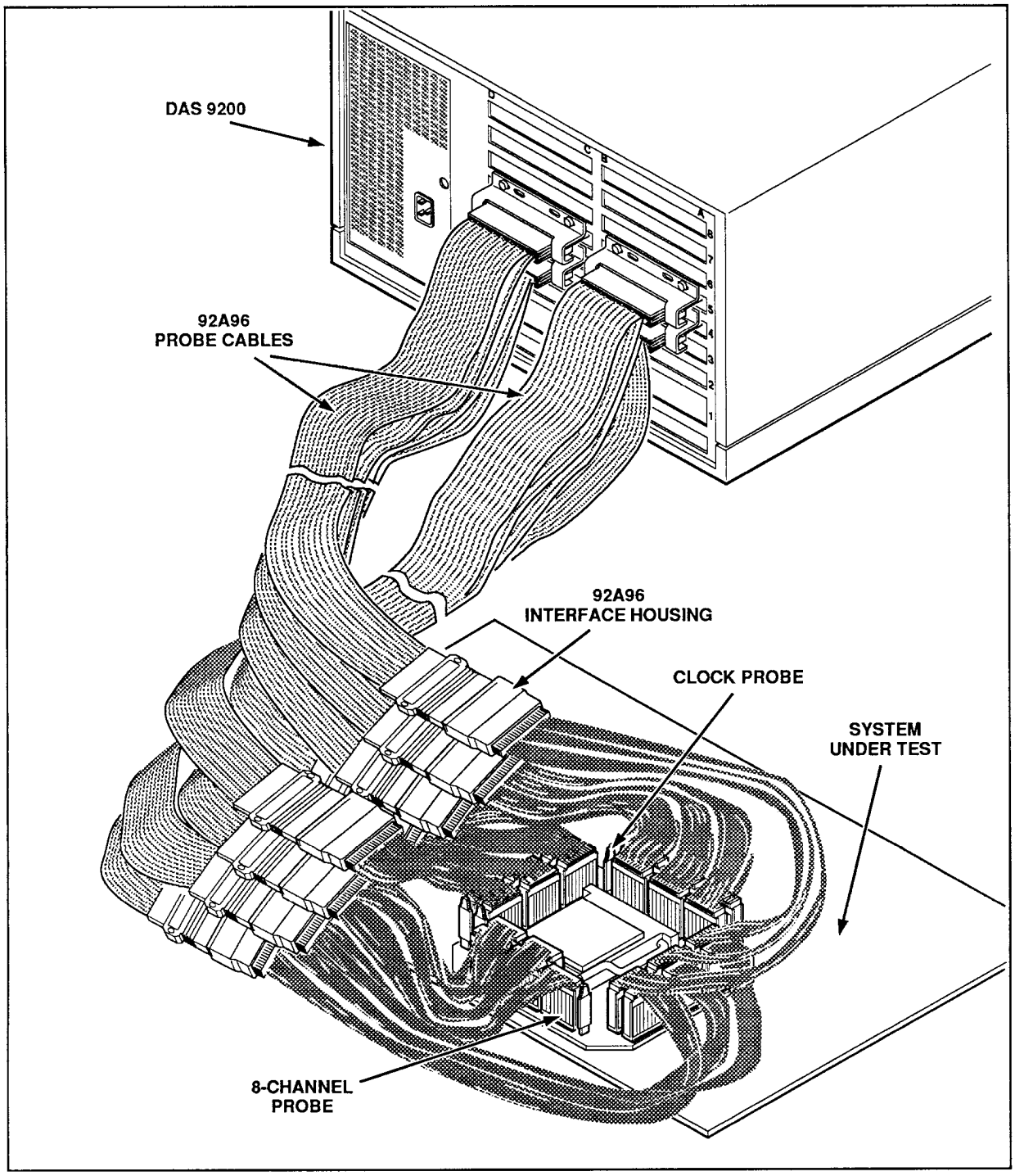

Figure 1-2. Overview of a DAS 9200 with two 92A96 Modules connected to an Am29000/050 system.

DIFFERENCES BETWEEN THE 92A96 AND 92A60/90 MODULES

If you have used a DAS 9200 with a 92A60/90 Module but haven't used a 92A96 Module, there are some key differences you should note. Table 1-1 lists the key differences.

Table 1-1
Differences Between 92A96 and 92A60/90 Data Acquisition Modules

Characteristic	92A96 Module	92A60/90 Module
Maximum synchronous data sampling rates	100 MHz	20 MHz
Maximum asynchronous data sampling rates	400 MHz, 24 channels or 200 MHz, 48 channels or 100 MHz, 96 channels	20 MHz, 60 or 90 channels
Memory depth	92A96 has 8K 92A96D has 32K	92A90 has 32K 92A90D has 128K
Physical connections to the probe adapter	4 probe cables connecting to 1 clock probe and three 8-channel probes each	2 or 3 cables connecting to 1 buffer probe
Clock channels	Not stored as data	Stored as data
Clock Menu selections	Custom, Internal, External	Micro, Demux, Internal, External
Flags	1 flag	2 flags
Counter/timers	2 counter/timers	3 counter/timers
Counter/timer width	32-bit counter/timer	24-bit counter/timer
Word/range recognizers	8 word and 0 range or 6 word and 1 range or 4 word and 2 range	8 word and 2 range

Am29000/050 SYSTEM REQUIREMENTS AND RESTRICTIONS

You should consider certain system requirements and restrictions of the Am29000/050 microprocessor before operating the disassembler. You should also consider all electrical, environmental, and mechanical specifications in Appendix B as they pertain to your system under test. The remainder of this section describes other Am29000/050 constraints.

System Clock Rate. The microprocessor support package supports the Am29000/050 microprocessor running up to 33 MHz[1].

[1] Specification at time of printing. Contact your DAS 9200 sales representative for current information on the fastest devices supported.

Hardware Reset. If a hardware reset occurs in your Am29000/050 system during an acquisition, the 92DM72A may acquire an invalid sample.

Branch Target Cache. The disassembler may not acquire some instructions if the Branch Target Cache is enabled. Therefore, if the Branch Target Cache is enabled, acquired data will be missing these instructions since they are not visible on the bus. Refer to the description of the *Branch Target Cache* in Section 4 for details on how data is displayed with the cache enabled and disabled.

Probe Adapter Clearance. Your Am29000/050 system must have a minimum amount of clear space surrounding the Am29000/050 microprocessor to accommodate the probe adapter. Figure C-1 in *Appendix C: Service Information* shows these minimum clearances.

Am29000/050 System and Probe Adapter Cooling. You must be sure to retain the original level of cooling inside your Am29000/050 system after the probe adapter is installed. You may also want to consider additional cooling for the probe adapter.

Probe Loading. Any electrical connection to your system adds an additional ac and dc load. The 92A96 Module probes and 92DM72A probe adapter were carefully designed to add the minimum possible load to your system. This additional load may affect the operation of the Am29000/050 system in systems with extremely tight timing margins. Appendix C contains complete specifications on how the 92DM72A probe adapter affects your system. If loading from the sockets is a problem, remove the ZIF socket first. If loading is still a problem, you can remove the protective socket from the underside of the probe adapter. Refer to the discussion on *Removing and Replacing Sockets* in Appendix C for directions on how to do this.

Section 2: QUICK START

If you are an experienced user of 92A60, 92A90, or 92A96 Data Acquisition Modules, you can use this section to quickly set up your system and use it. Before setting up your system, read the discussion on *Am29000/050 System Requirements and Restrictions* in Section 1.

Symbol tables are presented at the end of this section for you to remove or photocopy. This provides you with an easy reference when setting up the Trigger menu using symbols. All of the symbol tables are duplicated in Section 3 in case they are lost or damaged after being removed.

CONFIGURING THE DAS 9200

You must make sure that the data acquisition modules are positioned correctly in the DAS 9200 in order for disassembly to be correct. When using the supplied cluster setup, the module in the lower-numbered slot acquires data from the code bus and is called the C_Bus module. The module in the higher-numbered slot acquires data from the data bus and is called the D_Bus module.

When using two 92A96 Modules, they must be positioned next to each other in the DAS 9200. Probe cables should be connected to the modules after you position the modules. Directions for connecting the probe cables and positioning the modules are in the module user's manual. In a multimodule system, it is easier to identify which modules are connected to the probe adapter if slot number labels are applied to the module and DAS 9200. Figure 2-1 shows how to apply slot number labels.

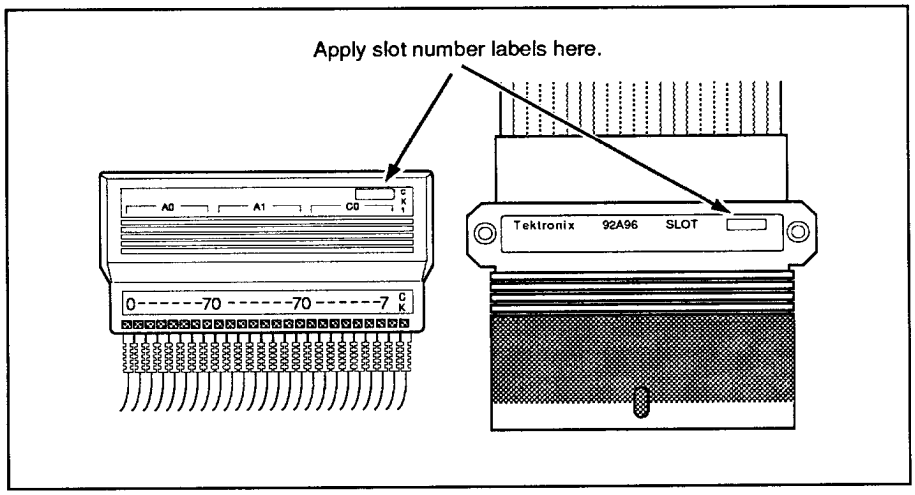

Figure 2-1. Applying slot number labels.

INSTALLING SOFTWARE

The DAS 9200 will not allow you to install 92DM72A software if 92DM72 software is already installed on the system. The DAS 9200 will not overwrite 92DM72 files with 92DM72A files. Therefore, you will have to remove 92DM72 software prior to installing 92DM72A software.

However, the DAS 9200 will overwrite 92DM72A files if you reinstall 92DM72 software. Be aware of this if you need to reinstall 92DM72 on a system that already has 92DM72A software installed on it.

To install the Am29000/050 support software, follow these steps:

1. Power on the DAS 9200 and select the Disk Services menu.
2. Select Install Application and press F8: EXECUTE OPERATION.
3. Follow the on-screen prompts.

You may need to remove applications or files from the hard disk if there is not enough available disk free space to accommodate the microprocessor support files.

CONFIGURING THE PROBE ADAPTER

The Am29000/050 microprocessor lets you select either Big- or Little-Endian byte ordering for data reads and writes. A byte-order jumper on the probe adapter must be used to set the default byte ordering used for disassembly when you power up the DAS 9200 and Am29000/050. You should set the jumper to match the byte ordering normally used in your Am29000/050 system.

Set the jumper in the B position to acquire data using Big-Endian byte ordering; set it in the L position to acquire data using Little-Endian byte ordering. Setting the jumper to B is the same as initializing bit 2 of the Byte Order (BO) bus for the Am29000/050 configuration register to 0.

Figure 2-2 shows the location of the byte-order jumper on the probe adapter.

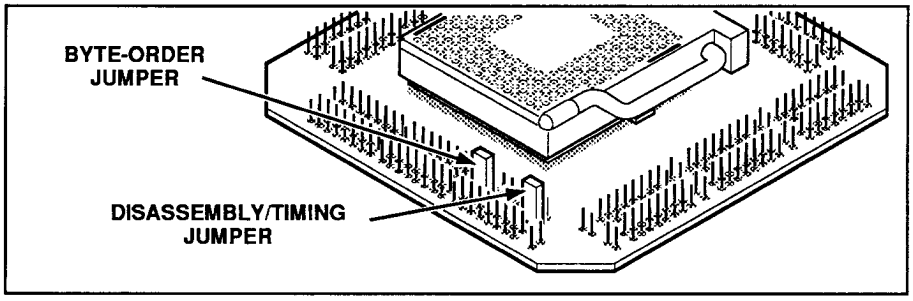

Figure 2-2. Location of the byte-order and disassembly/timing jumpers on the probe adapter.

You can also change the byte ordering used for disassembly between acquisitions; use the Data Byte Order field of the Disassembly Format Definition overlay. Refer to the description of the *Disassembly Format Definition Overlay* in Section 4 for details on how to do this.

The disassembly/timing jumper is used in conjunction with clocking selections in the Clock menu. Custom and External clocking sets the 92A96 Module to sample data based on an external clock, in this case, the system clock of the Am29000/050. This type of sampling is commonly called synchronous. Internal clocking sets the 92A96 to sample data based on a clock internal to that module and is commonly called asynchronous.

The jumper must be set in the D position when sampling data synchronously with the Am29000/050 system. Disassembly will only be correct when this jumper is in the D position. You can also view acquired data using Internal clocking (asynchronous) with the jumper in the D position, but no data will be seen for the SYSCLK signal. In the D position, the SYSCLK signal, the Am29000/050 system clock signal, is used as a sampling clock source and is not stored as data.

You can set the jumper in the T position when sampling data asynchronously using Internal clocking. The SYSCLK signal is acquired as data and can be viewed in the display menus.

CONNECTING THE DAS 9200 TO THE Am29000/050 SYSTEM

You can connect a single 92A96 Module to acquire data from just the code or the data bus, or two modules to acquire data from both buses. When acquiring data from both buses, the C_Bus module is positioned in the lower-numbered slot and the D_Bus module is positioned in the higher-numbered slot. You should

make all the clock and 8-channel probe connections as shown in Figures 2-5 and 2-7 when using two modules.

CAUTION

Static-discharge can damage the Am29000/050 microprocessor, clock probes, 8-channel probes, or the 92A96 Module. To prevent static damage, observe the following precautions while following all the connection procedures.

Handle the microprocessor only in a static-free environment.

Always wear a grounding wrist strap, or similar device, while handling the microprocessor and probe adapter.

If the 92A96 Module probe cables are not already connected to the interface housings, refer to Figure 2-3 and follow this procedure:

1. Match the color of the label and slot number on the interface housing to the color of the label and slot number on the loose end of a 92A96 probe cable.
2. Line up the key and key slot and connect them.
3. Repeat steps 1 and 2 for the remaining interface housings and probe cables (three for a single module or seven for two modules).

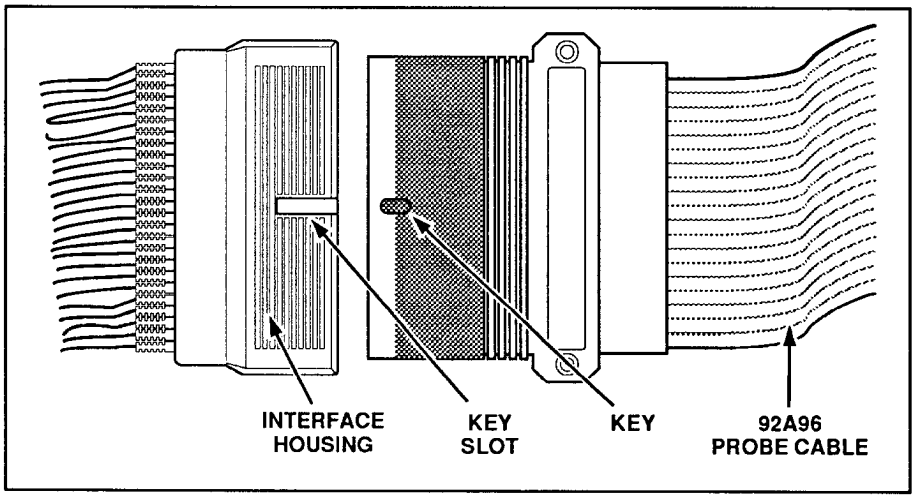

Figure 2-3. Connecting the interface housing to the 92A96 probe cable. The label on the interface housing is not on the side with the key slot.

To connect the clocks and 8-channel probes from the C_Bus module to the probe adapter, follow this procedure:

1. Use the antistatic shipping material to support the probe adapter when connecting the clock and 8-channel probes as shown in Figure 2-4. This prevents the circuit board from being flexed and socket pins from being bent.

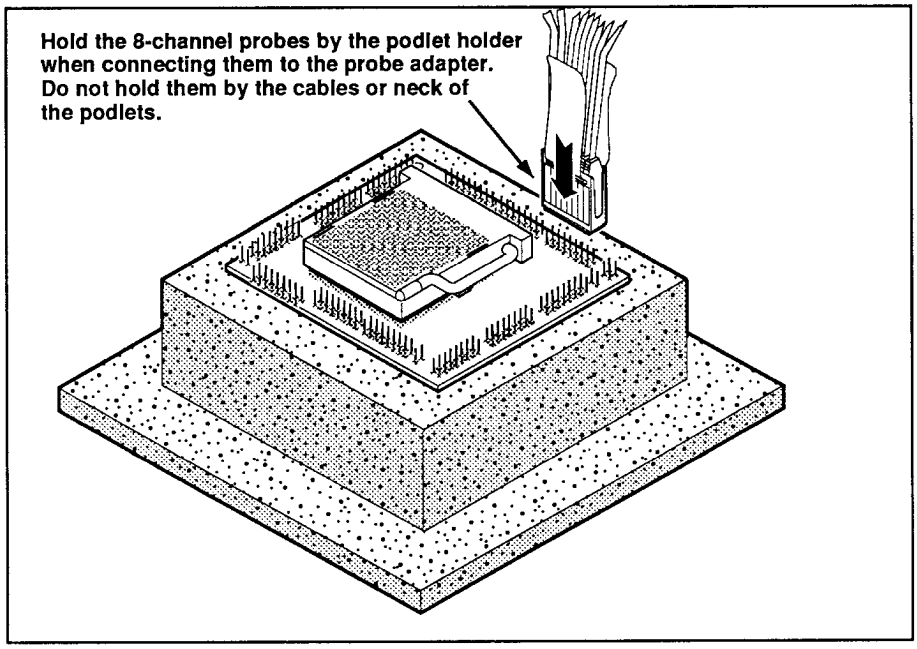

Figure 2-4. Connecting clock and 8-channel probes to the probe adapter.

2. Match the section names and channel numbers on the interface housings to the probe adapter as shown in Figure 2-5. Sections that connect to the code bus have a C- preceding the section name on the probe adapter, such as C-A0, C-A1, and so on. Be sure to match the clock and 8-channel probes from the C_Bus module when using two modules.

NOTE

Connect only the signal connectors to the signal pins and the ground connectors to the ground pins. Connecting any Am29000/050 signal to a probe adapter ground pin can cause the Am29000/050 microprocessor to malfunction.

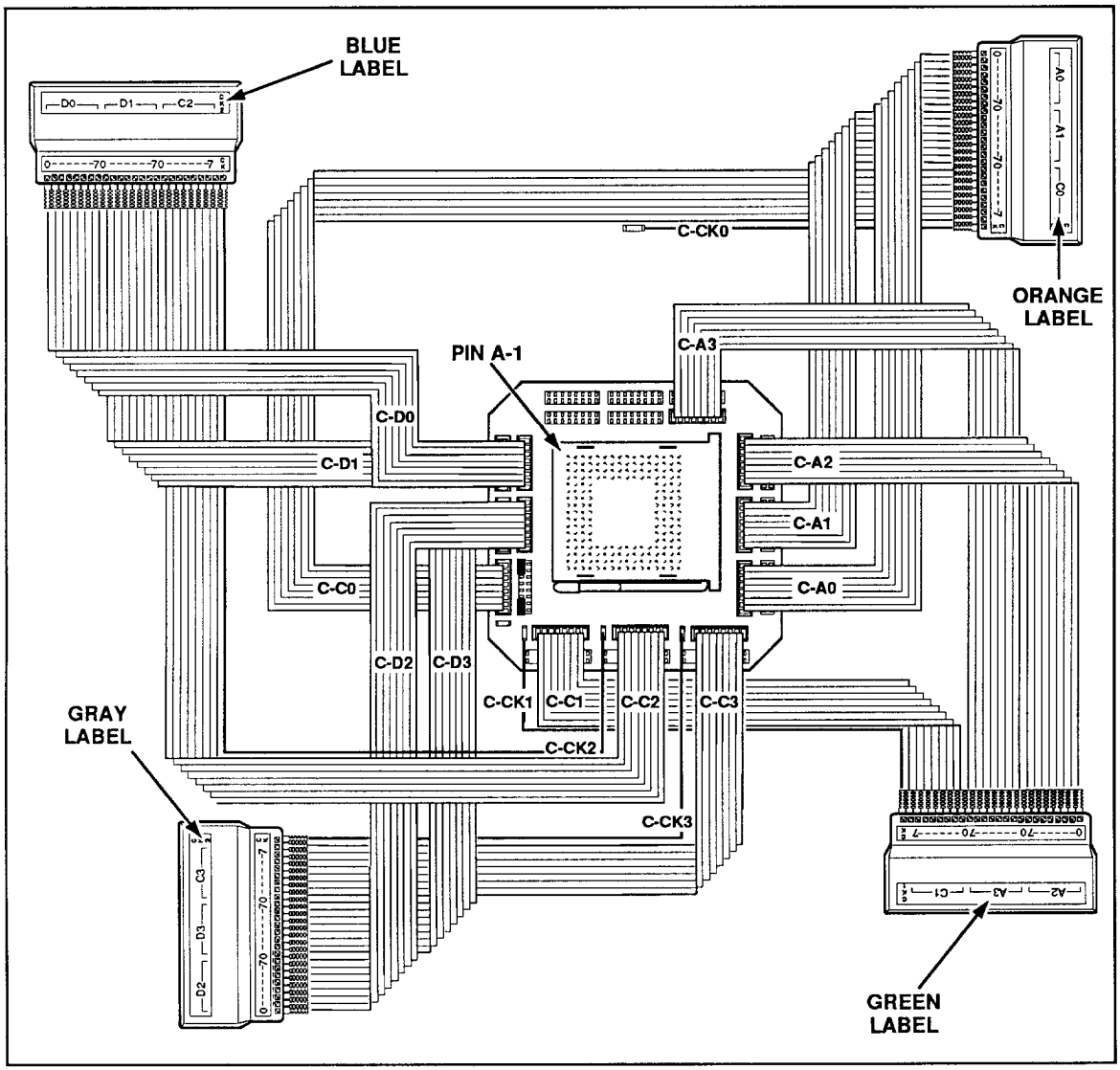

Figure 2-5. Connections from the C_Bus module probes to the probe adapter. Clock 0 of the C_Bus module (C-CK0) does not connect to the probe adapter.

3. Connect the clocks and 8-channel probes to the appropriate sets of square pins on the probe adapter.

   If you are connecting four or more adjacent 8-channel probes to the probe adapter, refer to Figure 2-6 and connect the 8-channel probes in the following order:

   a. Connect two 8-channel probes one at a time on the outside groups of square pins on any one side of the probe adapter.

   b. Align and start to connect the center pair of 8-channel probes on the remaining two groups of square pins.

c. Hold the center two 8-channel probes together as one 16-channel probe and push them onto the square pins.

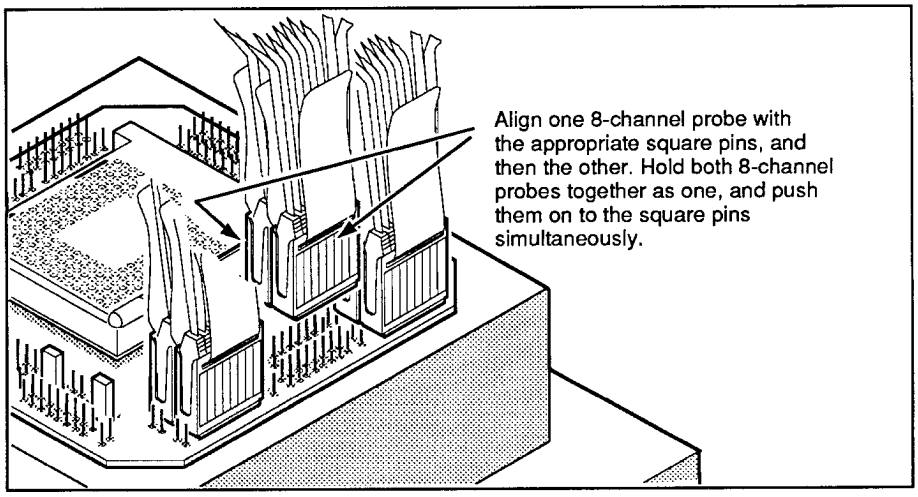

Figure 2-6. Connecting six adjacent 8-channel probes.

To connect the clocks and 8-channel probes from the D_Bus module to the probe adapter, refer to Figure 2-7 and follow the previous procedure.

Match the section names and channel numbers on the interface housings to the probe adapter. Sections that connect to the data bus have a D- preceding the section name on the probe adapter, such as D-A0, D-A1, and so on. Be sure to match the clock and 8-channel probes from the D_Bus module when using two modules.

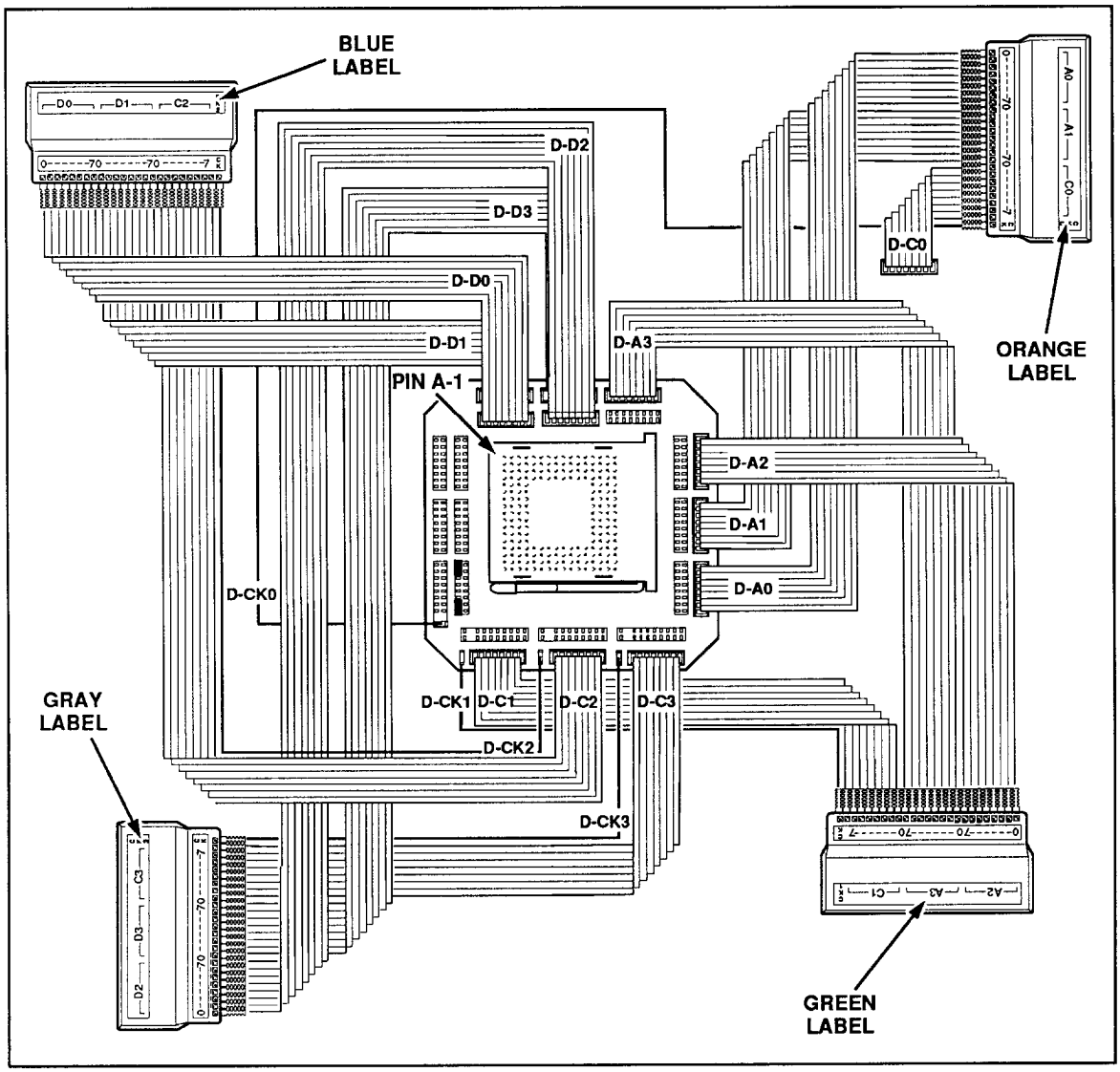

Figure 2-7. Connections from the D_Bus module probes to the probe adapter. Section C0 of the D_Bus module (D-C0) does not connect to the probe adapter.

To connect the probe adapter to the system under test, refer to Figure 2-8 and follow this procedure:

1. Power down your Am29000/050 system and carefully remove the microprocessor. (It is not necessary to power down the DAS 9200.) Be sure to follow standard static precautions while handling either the microprocessor or the probe adapter. These precautions are detailed in Section 3.
2. Carefully plug the probe adapter into the Am29000/050 socket. Align pin A-1 on the probe adapter to pin A-1 on the Am29000/050 system socket.

CAUTION

You can damage the microprocessor, the sockets on the probe adapter, and the system socket if you do not properly orient the Am29000/050. A-1 is printed on the circuit board. The Am29000/050 microprocessor also has a keying pin, number 169, to ensure proper alignment of pin A-1. Figure 2-8 shows the proper alignment of pin A-1 on the microprocessor, the ZIF socket, and the Am29000/050 system socket.

3. Open the ZIF socket by pulling the lever up and away from the socket.
4. Carefully plug the Am29000/050 microprocessor into the ZIF socket. Align pin A-1 on the Am29000/050 to pin A-1 of the socket.
5. Push the ZIF socket's lever down to lock the ZIF socket.

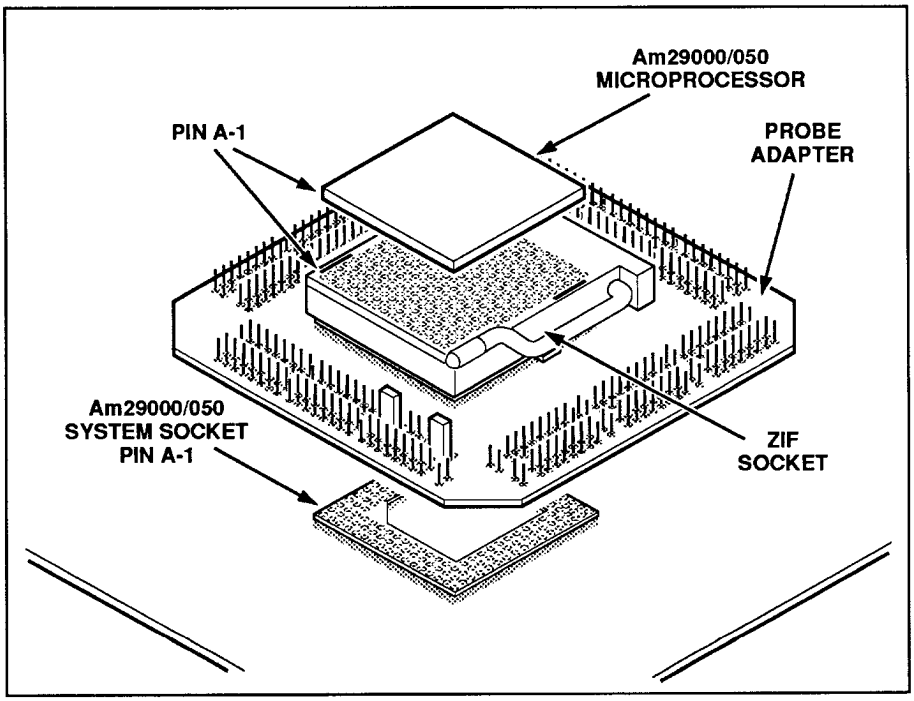

Figure 2-8. Placing the probe adapter in the Am29000/050 system. The clock and 8-channel probes should already be connected before placing the probe adapter in the system. They are not shown connected in this figure because they obscure the detail.

SETTING UP THE DISASSEMBLER

To set up the disassembler, perform the following steps:

1. If you are using two modules, restore the cluster setup provided with the disassembler software. Select the Save/Restore menu and select Restore Setup in the Operation field. Open the File field and select the 29000_9696 file.

   Press F8: EXECUTE OPERATION. When you do this, the Channel, Clock, and Trigger menus for both the C_Bus and D_Bus modules will be set up for microprocessor support.

   If you are using one module, access the Configuration menu and select 29000C Support or 29000D Support in the Software Support field. When you do this, the Channel, Clock, and Trigger menus for the C_Bus or D_Bus module will be set up for microprocessor support.

   Two or three 92A96 Modules in adjacent slots are automatically formed into a multicard module by the system software at power-up. If you need to use one 92A96 Module from a multicard module, you must reconfigure the DAS 9200 accordingly prior to selecting software support in the 92A96 Configuration menu. If you restore a supplied cluster setup, the reconfiguration is done for you. Refer to the discussion of the System Configuration menu in the *DAS 9200 System User's Manual* for details on how to reconfigure multicard modules.

   NOTE

   Remember to read the discussion Am29000/050 System Requirements and Restrictions *in Section 1 prior to setting up the 92A96 Module or Modules for disassembly.*

   Do not disturb the C_Addr, C_Data, C_Ctrl or C_Intr groups for the C_Bus module (in the Channel menu), the D_Addr, D_Data, D_Ctrl groups for the D_Bus module (in the Channel menu), or the channel assignments within them while using the disassembler. Changing these groups causes invalid instruction mnemonics disassembly. You can find the channel group definitions and channel assignments in Appendix C.

2. If you want to include DMA cycles, you will have to change the Custom clocking DMA Cycles option in the Clock menu for the D_Bus module. The DMA Cycles option is not available for the C_Bus module. The default for Custom clocking for the D_Bus module is to exclude DMA cycles. Refer to Appendix B for a description of how DMA cycles are acquired.
3. If you are performing hardware analysis, you can select Internal or External clocking in the Clock menu. Mnemonic disassembly may be invalid with either of these clocking modes.
4. Select the Trigger menu if you want to change the trigger program. The default trigger program will trigger on the first data sample acquired after pressing F1: START.

Tables 2-1 through 2-3 are symbol tables intended for you to remove or photocopy and use while performing disassembly.

ACQUIRING AND DISPLAYING DATA

After completing the DAS 9200 and probe adapter setups, you can acquire and display data. To acquire and view instruction mnemonics, perform the following steps:

1. Press F1: START on the DAS 9200 from any setup or display menu.
2. Power on and start running the Am29000/050 system. (You can also power on the Am29000/050 system before pressing F1: START on the DAS 9200.)

   After satisfying the trigger program and filling acquisition memory, the DAS 9200 will display data in the default State menu. You may need to press F1: STOP if the stop conditions are not met.
3. Select the Disasm menu from the Menu Selection overlay to view instruction mnemonics.
4. To disassemble data from an Am29050 microprocessor, select 29050 in the Processor Choice field of the Disassembly Format Definition overlay. Disassembly for the Am29000 is the default selection in this field.
5. If you are performing hardware analysis (Internal or External clocking), select the Timing menu from the Menu Selection overlay to view timing data. You can use the default State menu to view state data for hardware analysis.

The Disassembly menu displays the disassembled data in different formats:

- Hardware format shows instruction mnemonics on Fetch cycles and cycle-type information for all other cycles.
- Software format shows only opcode fetches; all other cycle types are suppressed.
- Control Flow format shows only instructions that change the control flow.
- Subroutine format shows only subroutine calls, and interrupt/trap calls and returns.

Refer to *Appendix A: Error Messages and Disassembly Problems* if there are problems acquiring either instruction mnemonics or timing data.

This is the end of the *Quick Start* section.

Table 2-1
C_Ctrl Group Symbol Table (29000C_Ctrl)

Symbol	C_Ctrl Group Value *IREQ *IRDY IREQT SUP/*US *LOCK *RESET *IERR *BINV	Meaning
SUP_LOCK	X 0 X 1 0 1 1 1	The Am29000/050 is operating in Supervisor mode and the *LOCK signal is asserted
USER_LOCK	X 0 X 0 0 1 1 1	The Am29000/050 is operating in User mode and the *LOCK signal is asserted
LOCK	X 0 X X 0 1 1 1	A cycle in which the *LOCK signal is asserted
SUP	X 0 X 1 X 1 1 1	The Am29000/050 is operating in Supervisor mode
USER	X 0 X 0 X 1 1 1	The Am29000/050 is operating in User mode
FETCH_ROM	X 0 1 X X 1 1 1	A cycle in which an instruction fetch from ROM occurred
FETCH_RAM	X 0 0 X X 1 1 1	A cycle in which an instruction fetch from RAM occurred
FETCH	X 0 X X X 1 1 1	A cycle in which an instruction fetch occurred
RESET	X X X X X 0 X X	A cycle in which the *RESET signal is asserted
IERR_IDLE	X X X X X 1 0 0	A cycle that both the Am29000/050 and the slave device determined is an invalid access
IERR	X X X X X 1 0 X	A cycle that the slave device determined is an invalid access
IDLE	X X X X X 1 X 0	A cycle that the Am29000/050 determined is an invalid access

Table 2-2
C_Intr Group Symbol Table (29000C_Intr)

Symbol	C_Intr Group Value *WARN *TRAP1 *TRAP0 *INTR3 *INTR2 *INTR1 *INTR0	Meaning
WARN	0 X X X X X X X	A non-maskable *WARN trap that bypasses the normal trap vector fetch sequence
TRAP0	1 X 0 X X X X X	Highest priority TRAP request
TRAP1	1 0 X X X X X X	Lowest priority TRAP request

(Cont.)

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Table 2-2 (Cont.)
C_Intr Group Symbol Table (29000C_Intr)

Symbol	C_Intr Group Value *WARN *TRAP1 *TRAP0 *INTR3 *INTR2 *INTR1 *INTR0	Meaning
INTR0	1 X X X X X 0	Highest priority external interrupt
INTR1	1 X X X X 0 X	Second highest priority external interrupt
INTR2	1 X X X 0 X X	Second lowest priority external interrupt
INTR3	1 X X 0 X X X	Lowest priority external interrupt
NONE	1 1 1 1 1 1 1	No pending interrupt

Table 2-3
D_Ctrl Group Symbol Table (29000D_Ctrl)

Symbol	D_Ctrl Group Value B/*L R/*W *BGRT DREQT1 DREQT0 OPT2 OPT1 OPT0 SUP/*US *LOCK *RESET *DERR *BINV	Meaning
READ_SUP	X 1 1 0 0 X X X 1 X 1 1 1	A read from memory that occurs when the Am29000/050 is operating in Supervisor mode
WRITE_SUP	X 0 1 0 0 X X X 1 X 1 1 1	A write to memory that occurs when the Am29000/050 is operating in Supervisor mode
INPUT_SUP	X 1 1 0 1 X X X 1 X 1 1 1	A read from an I/O device that occurs when the Am29000/050 is operating in Supervisor mode
OUTPUT_SUP	X 0 1 0 1 X X X 1 X 1 1 1	A write to an I/O device that occurs when the Am29000/050 is operating in Supervisor mode
READ_USER	X 1 1 0 0 X X X 0 X 1 1 1	A read from memory that occurs when the Am29000/050 is operating in User mode
WRITE_USER	X 0 1 0 0 X X X 0 X 1 1 1	A write to memory that occurs when the Am29000/050 is operating in User mode
INPUT_USER	X 1 1 0 1 X X X 0 X 1 1 1	A read from an I/O device that occurs when the Am29000/050 is operating in User mode
OUTPUT_USER	X 0 1 0 1 X X X 0 X 1 1 1	A write to an I/O device that occurs when the Am29000/050 is operating in User mode
READ_LOCK	X 1 1 0 0 X X X X 0 1 1 1	A read from memory that occurs when the *LOCK signal is asserted

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Table 2-3 (Cont.)
D_Ctrl Group Symbol Table (29000D_Ctrl)

Symbol	D_Ctrl Group Value B/*L R/*W *BGRT DREQT1 DREQT0 OPT2 OPT1 OPT0 SUP/*US *LOCK *RESET *DERR *BINV	Meaning
WRITE_LOCK	X 0 1 0 0 X X X X 0 1 1 1	A write to memory that occurs when the *LOCK signal is asserted
INPUT_LOCK	X 1 1 0 1 X X X X 0 1 1 1	A read from an I/O device that occurs when the *LOCK signal is asserted
OUTPUT_LOCK	X 0 1 0 1 X X X X 0 1 1 1	A write to an I/O device that occurs when the *LOCK signal is asserted
READ	X 1 1 0 0 X X X X X 1 1 1	A read to memory
WRITE	X 0 1 0 0 X X X X X 1 1 1	A write from memory
INPUT	X 1 1 0 1 X X X X X 1 1 1	A read to an I/O device
OUTPUT	X 0 1 0 1 X X X X X 1 1 1	A write from an I/O device
SUP_LOCK	X X X X X X X X 1 0 1 1 1	The Am29000/050 is operating in Supervisor mode and the *LOCK signal is asserted
USER_LOCK	X X X X X X X X 0 0 1 1 1	The Am29000/050 is operating in User mode and the *LOCK signal is asserted
LOCK	X X X X X X X X X 0 1 1 1	A cycle in which the *LOCK signal is asserted
SUP	X X X X X X X X 1 X 1 1 1	The Am29000/050 is operating in Supervisor mode
USER	X X X X X X X X 0 X 1 1 1	The Am29000/050 is operating in user mode
RESET	X X X X X X X X X X 0 X X	A cycle in which the *RESET signal is asserted
DERR_IDLE	X X X X X X X X X X 1 0 0	A cycle that the Am29000/050 and the slave device determined as an invalid access
DERR	X X X X X X X X X X 1 0 X	A cycle that the slave device determined as an invalid access
IDLE	X X 1 X X X X X X X 1 X 0	A cycle that the Am29000/050 determined as an invalid access
DMA_CYCLE	X X 0 X X X X X X X X X 1	A cycle in which a DMA occurs
BUS_GRANT	X X 0 X X X X X X X X X 0	A cycle in which control of the bus is granted to another device

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Section 3: INSTALLATION AND CONNECTIONS

This section contains detailed descriptions of how to do the following:

- configure the DAS 9200
- position the modules in the DAS 9200
- install the disassembler software
- view the demonstration reference memories
- configure the probe adapter
- set up the disassembler software
- connect the DAS 9200 to the system under test (SUT)

You can install the software either before or after installing the modules or connecting the probe adapter to the Am29000/050 system. The jumpers can also be changed at any time.

CONFIGURING THE MODULES

Included with the microprocessor support software are three setups that simplify preparation when you are acquiring Am29000/050 data. Two are single module setups and one is a multimodule setup. You can also create your own setups and save them for later use. This discussion describes the setups provided with the disassembler, the requirements for using these setups, and creating your own setups.

If you are using two modules, they must be positioned next to each other in the DAS 9200 for disassembly to be correct. The module in the lower-numbered slot is the C_Bus module and acquires data from the code bus. The module in the higher-numbered slot is the D_Bus module and acquires data from the data bus.

INSTALLING SOFTWARE

The disassembler software sets up the DAS 9200 to acquire, disassemble, and display data from an Am29000/050 system. To install the software, the application files on the 5 1/4-inch floppy disk must be copied to the DAS 9200 hard disk. You cannot execute the disassembler from the floppy disk.

The DAS 9200 will not allow you to install 92DM72A software if 92DM72 software is already installed on the system. The DAS 9200 will not overwrite 92DM72 files with 92DM72A files. Therefore, you will have to remove 92DM72 software prior to installing 92DM72A software.

However, the DAS 9200 will overwrite 92DM72A files if you reinstall 92DM72 software. Be aware of this if you need to reinstall 92DM72 on a system that already has 92DM72A software installed on it.

To install the software, follow these steps:

1. Power on the DAS 9200 and press the Select Menu key.
2. Select the Disk Services menu in the Utilities column.
3. Press the Return key.
4. Select Install Applications in the Operation field.
5. Press F8: EXECUTE OPERATION and follow the on-screen prompts.

If there is inadequate disk free space available on the hard disk, you must use the Remove Application or Delete File function of the Disk Services menu to free up enough disk space to install the software. The approximate space required to install the software is listed on the label of the 92DM72A floppy disk.

After the DAS 9200 successfully copies the application files from the floppy disk to the hard disk, the message **Application installation complete with no errors** appears on your screen. Remove the floppy disk and store it in a safe place in case you need to reinstall the software.

If you would like to see an example of Am29000/050 bus activity with mnemonic disassembly, read the next discussion and procedure.

Viewing the Refmem File

Two reference memory files are provided for you to familiarize yourself with the way the disassembler displays Am29000 and Am29050 cycle types and instruction mnemonics. You can select the reference memory file to see how Am29000 or Am29050 mnemonics are displayed without making any of the DAS 9200 connections to your system under test.

The 29000_Demo and 29050_Demo reference memory files are automatically installed when the disassembler software is installed on the hard disk. A symbol table file for the C_Addr group (called 29000_Demo) is also automatically installed and is valid only for the 29000_Demo reference memory file. Most of the figures in Section 4 showing acquired data are from these files. The data you acquire from your Am29000/050 system will be different.

To view the 29000_Demo or 29050_Demo Refmem, use the following procedure:

1. Press the Select Menu key to return to the Menu Selection overlay.
2. Move the cursor to the Refmem column and select the 29000_Demo or 29050_Demo file.
3. Move the cursor to the Display column and select Disasm.
4. Press the Return key to view the reference memory.

   To correctly display the vector table for this reference memory, refer to the description on *Defining and Using the Vector Area* in Section 4.

You can change the format of disassembled data from the Disassembly Format Definition overlay, which you can access through the Disassembly menu. Hardware disassembly is the default format in the Disassembly menu. Examples of the disassembly formats are found under *Display Formats* in Section 4.

If there is not enough free space left on the hard disk, you can delete the 29000_Demo and 29050_Demo files. They are presented strictly for viewing and are not necessary to the operation of the disassembler.

Setting Up Disassembler Software

The microprocessor support package supplies the disassembler software and setup files for the data acquisition module to use to acquire and display instruction mnemonics. Setup files are supplied for the Channel, Clock, and Trigger menus. Symbol files are supplied for displaying data and to use in the Trigger menu as word recognizer values. Format files are also provided for the Timing menu when performing hardware analysis (described in Section 5).

Before selecting and setting up the disassembler, read the descriptions of *Am29000/050 System Requirements and Restrictions* in Section 1.

You can select the disassembler and its associated setup files by restoring the supplied cluster setup file. Refer to the procedure in *Restoring and Using a Multimodule Setup* later in this section.

When there are two or three 92A96 Modules in adjacent slots, they are automatically formed into a multicard module by the system software at power up. If you need to use one 92A96 Module from a multicard module, you must reconfigure the DAS 9200 accordingly prior to selecting software support in the 92A96 Configuration menu. If you restore a supplied cluster setup, the reconfiguration is done for you. Refer to the discussion of the System Configuration menu in the *DAS 9200 System User's Manual* for details on how to reconfigure multicard modules.

Single Module Setup

If you are using one module, access the Configuration menu and select 29000C Support or 29000D Support in the Software Support field. When you do this, the Channel, Clock, and Trigger menus for the C_Bus or D_Bus module will be set up for microprocessor support.

When you select 29000C or 29000D Support in the Configuration menu of a single unclustered 92A96 Module, single module setup files are provided for disassembly. The 29000C setup configures the DAS 9200 to acquire data only from the code bus of the Am29000/050. The 29000D setup configures the DAS 9200 to acquire data only from the data bus of the Am29000/050.

Multimodule Setup

When you select a multimodule setup the DAS 9200 automatically will do the following:

- cluster and correlate two 92A96 Modules
- designate the module in the lower-numbered slot as the C_Bus module and the module in the higher-numbered slot as the D_Bus module
- select the appropriate software support for each module
- define two communication signals for use in the trigger programs of the modules called C-to-D and D-to-C
- define triggering for each module using the communication signal C-to-D
- provide a predefined Timing Format Definition file, called 29000_9696, for the module cluster

The clustered module setup file provided with the disassembler software is called 29000_9696. The 29000_9696 setup configures the DAS 9200 to acquire data from both the code and data buses of an Am29000/050 system using two 92A96 Modules.

If both modules are not the same memory depth, the deeper module should be used as the C_Bus module and the shallower module should be used as the D_Bus module.

Restoring and Using a Multimodule Setup

To restore and use a multimodule setup, refer to Figure 3-1 and follow these steps:

1. Select the Save/Restore menu.
2. Press the Return key.
3. Select Restore Setup in the Operation field.
4. Select the desired setup in the File field. The disassembler software supplies one cluster setup file called 29000_9696.
5. Press F8: EXECUTE OPERATION.

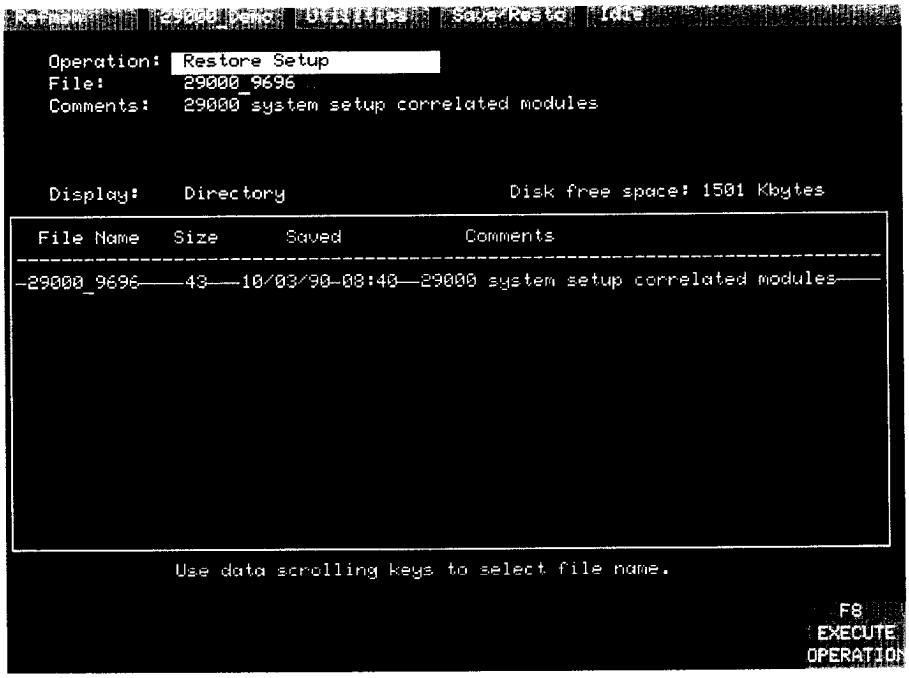


Figure 3-1. Save/Restore menu. The 29000_9696 multimodule setup listed in the directory is included with the disassembler software.

The DAS 9200 automatically configures itself for multimodule operation. If the current placement of the data acquisition modules does not match that of the setup selected, the Restore Formation overlay appears. Press the F4: PLACE MODULES key or use the overlay to assign the module setups to the current placement of the data acquisition modules. This applies to all versions of any data acquisition module.

If you are using 92A96D modules when you restore a setup, the 92A96D's default memory depth is set to 8K. To use a greater memory depth, select a higher value in the Acquisition Memory Size field of the Configuration menu for each deep module.

Creating Multimodule Setups

You can create new setups that meet the needs of your specific application. For example, you can create a setup that provides additional inter-module communication signals for use in more complex trigger programs, or a setup to acquire data from multiple Am29000/050 microprocessors.

To create a new setup using the Am29000/050 disassembler, you must first install the software and its associated files on your DAS 9200. Refer to the discussion on *Installing Software* in this section for directions on how to do this. After installing the software, you should select the pre-defined multimodule setup. If need be, you can change the setup, name the modified setup, and save it.

If you create a new cluster, certain naming conventions must be followed when naming the modules. You must use the names the disassembler assigned to the modules (C_Bus and D_Bus) but you can add a suffix. The same suffix must be used for each module for each Am29000/050 being disassembled; for example, C_BusNew and D_BusNew.

You must also correlate the data between the two modules. To correlate data from the two modules, refer to Figure 3-2 and use the following procedure:

1. Select the Cluster Setup menu from the Menu Selection overlay.
2. Press F4: DEFINE CORRELATN to access the Correlation Definition overlay.
3. Open the Correlate field, select the C_Bus module, and close the field.
4. Press F7: ADD CORR. A second field appears under the first.
5. Open the second field, select the D_Bus module, and close the field.
6. Press F8: EXIT & SAVE and return to the Menu Selection overlay to reconfigure the system with the C_Bus and D_Bus modules correlated.

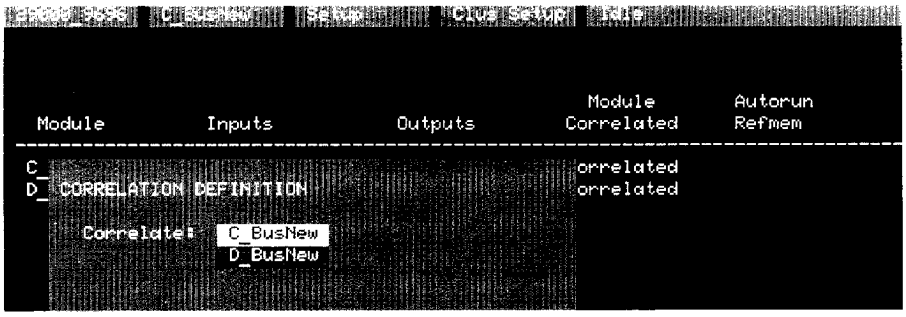


Figure 3-2. Correlation Definition overlay.

You must also define signals to use between two modules. To define signals for the two modules, refer to Figure 3-3 and use the following procedure:

1. Select the Cluster Setup menu from the Menu Selection overlay.
2. Press F2: DEFINE SIGNAL to access the Signal Definition overlay.
3. Press F7: ADD SIGNAL. A signal name field appears.
4. Enter the name of the signal and press Return.
5. Define the signals as either input or output in the Direction field and press Return.
6. Do not change the selection for the Type field.

   For information on any of these fields, refer to the *DAS 9200 System User's Manual.*
7. Press F8: EXIT & SAVE and return to the Menu Selection overlay to reconfigure the system with signals defined for correlated C_Bus and D_Bus modules.

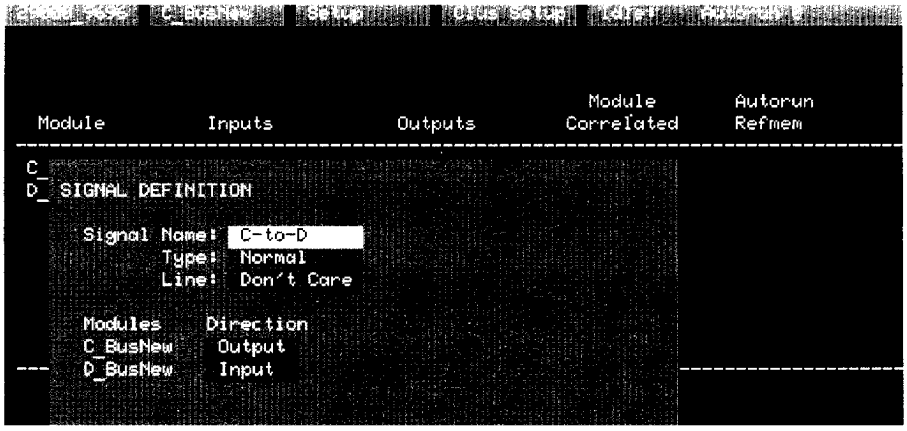


Figure 3-3. Signal Definition overlay.

To complete the setup, you must select 29000C Support for the C_Bus module and 29000D Support for the D_Bus module in the Configuration menu.

When two or three 92A96 Modules are in adjacent slots, they are automatically formed into a multicard module by the system software at power up. If you need to use two 92A96 Modules from a multicard module, you must reconfigure the DAS 9200 accordingly prior to selecting software support in the 92A96 Configuration menu. Refer to the discussion of the System Configuration menu in the *DAS 9200 System User's Manual* for details on how to reconfigure multicard modules.

Use the Save Cluster Setup operation of the Save/Restore menu to save the setup for later use.

What You Can Change During Setup

You can change part of the module setup without affecting disassembly. You can change the trigger program in the Trigger menu and the display radix for any channel group in the Channel menu. Any change to the radix of the D_Data group will only affect the Trigger and State menus, not the Disassembly menu. You can change the clocking selection for the DMA Cycles option field of the D_Bus module to Included or Excluded without affecting the disassembler.

You can change the channel grouping and name of the C_Intr, C_Aux1, C_Aux0, and D_Aux0 groups and not affect disassembly. You can also delete any of these groups.

You cannot change the channel grouping or the name of the C_Addr, C_Data, C_Ctrl, D_Addr, D_Data, and D_Ctrl groups, the threshold voltage, polarity, or clocking selection (Custom), and expect the disassembler to function properly.

You can connect the unused 8-channel probe to section C0 of the D_Bus module to other signals in your Am29000/050 system. You can also acquire data from any of the four Am29000/050 signals connected to a group of extra square pins on the probe adapter. Refer to the discussion on *Signals* in Appendix B for a list of these signal connections. Refer also to the discussion on *Alternate Connections* in this section for a description of how to make connections to other signals in your Am29000/050 system.

Channel Groups and Assignments

The disassembler relies on the presence of the signals and channel groups defined by the support software for the C_Addr, C_Data, and C_Ctrl channel groups of the C_Bus module and/or the D_Addr, D_Data, and D_Ctrl channel groups of the D_Bus module. Channel assignment tables are located in Appendix C.

Symbol Tables

You can use symbol tables to display channel group information symbolically in the State and Disassembly menus, and to control triggering.

The microprocessor support software contains symbol table files for the C_Ctrl, C_Intr, and D_Ctrl channel groups. The file names are 29000C_Ctrl, 29000C_Intr, and 29000D_Ctrl. These symbol tables assign symbolic names to combinations of signal values within the C_Ctrl, C_Intr, and D_Ctrl channel groups. Refer to *Displaying the C_Addr and D_Addr Groups Symbolically* in Section 4 for a description of how to display the C_Addr and D_Addr groups symbolically.

Table 3-1 shows the name, bit pattern, and meaning for the symbols in the file 29000C_Ctrl, the C_Ctrl group symbol table (control group for the C_Bus module).

Table 3-1
C_Ctrl Group Symbol Table (29000C_Ctrl)

Symbol	C_Ctrl Group Value *IREQ *LOCK *IRDY *RESET IREQT *IERR SUP/*US *BINV	Meaning
SUP_LOCK	X 0 X 1 0 1 1 1	The Am29000/050 is operating in Supervisor mode and the *LOCK signal is asserted
USER_LOCK	X 0 X 0 0 1 1 1	The Am29000/050 is operating in User mode and the *LOCK signal is asserted
LOCK	X 0 X X 0 1 1 1	A cycle in which the *LOCK signal is asserted
SUP	X 0 X 1 X 1 1 1	The Am29000/050 is operating in Supervisor mode
USER	X 0 X 0 X 1 1 1	The Am29000/050 is operating in User mode
FETCH_ROM	X 0 1 X X 1 1 1	A cycle in which an instruction fetch from ROM occurred
FETCH_RAM	X 0 0 X X 1 1 1	A cycle in which an instruction fetch from RAM occurred
FETCH	X 0 X X X 1 1 1	A cycle in which an instruction fetch occurred
RESET	X X X X X 0 X X	A cycle in which the *RESET signal is asserted
IERR_IDLE	X X X X X 1 0 0	A cycle that both the Am29000/050 and the slave device determined is an invalid access
IERR	X X X X X 1 0 X	A cycle that the slave device determined is an invalid access
IDLE	X X X X X 1 X 0	A cycle that the Am29000/050 determined is an invalid access

Table 3-2 shows the name, bit pattern, and meaning for symbols in the file 29000C_Intr, the C_Intr group symbol table (interrupt group for the C_Bus module).

Table 3-2
C_Intr Group Symbol Table (29000C_Intr)

Symbol	C_Intr Group Value *WARN *TRAP1 *TRAP0 *INTR3 *INTR2 *INTR1 *INTR0	Meaning
WARN	0 X X X X X X	A non-maskable *WARN trap that bypasses the normal trap vector fetch sequence
TRAP0	1 X 0 X X X X	Highest priority TRAP request
TRAP1	1 0 X X X X X	Lowest priority TRAP request
INTR0	1 X X X X X 0	Highest priority external interrupt
INTR1	1 X X X X 0 X	Second highest priority external interrupt
INTR2	1 X X X 0 X X	Second lowest priority external interrupt
INTR3	1 X X 0 X X X	Lowest priority external interrupt
NONE	1 1 1 1 1 1 1	No pending interrupt

Table 3-3 shows the name, bit pattern, and meaning for the symbols in the 29000D_Ctrl file, the D_Ctrl group symbol table (control group for the D_Bus module).

Table 3-3
D_Ctrl Group Symbol Table (29000D_Ctrl)

Symbol	D_Ctrl Group Value B/*L R/*W *BGRT DREQT1 DREQT0 OPT2 OPT1 OPT0 SUP/*US *LOCK *RESET *DERR *BINV	Meaning
READ_SUP	X 1 1 0 0 X X X 1 X 1 1 1	A read from memory that occurs when the Am29000/050 is operating in Supervisor mode
WRITE_SUP	X 0 1 0 0 X X X 1 X 1 1 1	A write to memory that occurs when the Am29000/050 is operating in Supervisor mode
INPUT_SUP	X 1 1 0 1 X X X 1 X 1 1 1	A read from an I/O device that occurs when the Am29000/050 is operating in Supervisor mode
OUTPUT_SUP	X 0 1 0 1 X X X 1 X 1 1 1	A write to an I/O device that occurs when the Am29000/050 is operating in Supervisor mode
READ_USER	X 1 1 0 0 X X X 0 X 1 1 1	A read from memory that occurs when the Am29000/050 is operating in User mode
WRITE_USER	X 0 1 0 0 X X X 0 X 1 1 1	A write to memory that occurs when the Am29000/050 is operating in User mode
INPUT_USER	X 1 1 0 1 X X X 0 X 1 1 1	A read from an I/O device that occurs when the Am29000/050 is operating in User mode
OUTPUT_USER	X 0 1 0 1 X X X 0 X 1 1 1	A write to an I/O device that occurs when the Am29000/050 is operating in User mode
READ_LOCK	X 1 1 0 0 X X X X 0 1 1 1	A read from memory that occurs when the *LOCK signal is asserted
WRITE_LOCK	X 0 1 0 0 X X X X 0 1 1 1	A write to memory that occurs when the *LOCK signal is asserted
INPUT_LOCK	X 1 1 0 1 X X X X 0 1 1 1	A read from an I/O device that occurs when the *LOCK signal is asserted
OUTPUT_LOCK	X 0 1 0 1 X X X X 0 1 1 1	A write to an I/O device that occurs when the *LOCK signal is asserted

(Cont.)

Table 3-3 (Cont.)
D_Ctrl Group Symbol Table (29000D_Ctrl)

Symbol	D_Ctrl Group Value B/*L R/*W *BGRT DREQT1 DREQT0 OPT2 OPT1 OPT0 SUP/*US *LOCK *RESET *DERR *BINV	Meaning
READ	X 1 1 0 0 X X X X X 1 1 1	A read to memory
WRITE	X 0 1 0 0 X X X X X 1 1 1	A write from memory
INPUT	X 1 1 0 1 X X X X X 1 1 1	A read to an I/O device
OUTPUT	X 0 1 0 1 X X X X X 1 1 1	A write from an I/O device
SUP_LOCK	X X X X X X X X 1 0 1 1 1	The Am29000/050 is operating in Supervisor mode and the *LOCK signal is asserted
USER_LOCK	X X X X X X X X 0 0 1 1 1	The Am29000/050 is operating in User mode and the *LOCK signal is asserted
LOCK	X X X X X X X X X 0 1 1 1	A cycle in which the *LOCK signal is asserted
SUP	X X X X X X X X 1 X 1 1 1	The Am29000/050 is operating in Supervisor mode
USER	X X X X X X X X 0 X 1 1 1	The Am29000/050 is operating in user mode
RESET	X X X X X X X X X X 0 X X	A cycle in which the *RESET signal is asserted
DERR_IDLE	X X X X X X X X X X 1 0 0	A cycle that the Am29000/050 and the slave device determined as an invalid access
DERR	X X X X X X X X X X 1 0 X	A cycle that the slave device determined as an invalid access
IDLE	X X 1 X X X X X X X 1 X 0	A cycle that the Am29000/050 determined as an invalid access
DMA_CYCLE	X X 0 X X X X X X X X X 1	A cycle in which a DMA occurs
BUS_GRANT	X X 0 X X X X X X X X X 0	A cycle in which control of the bus is granted to another device

Copying and Editing Predefined Symbol Tables

You cannot directly edit any symbol tables supplied by microprocessor support. But you can make a copy of a predefined symbol table and then edit the copy for your specific use.

To create a new symbol table, follow these steps:

1. Select the Symbol Editor menu.
2. Press F2: FILE FUNCTIONS.
3. Select Open File in the Function field.
4. Select New File in the Edit Status field.
5. Enter a new symbol table file name in the New File Name field.
6. Select Pattern in the Table Type field to match the symbol table you are copying.
7. Press F5: EXECUTE FUNCTION.
8. Select the Merge Files in the Function field.
9. Select the file to base your new symbol table on, such as the 29000C_Ctrl file, in the File Name to Merge In field.
10. Press F5: EXECUTE FUNCTION.
11. Press F8: EXIT & SAVE.
12. Edit the file as desired. Refer to your *DAS 9200 System User's Manual* for information on editing the symbol table.
13. Press the Select Menu key to return to the Menu Selection overlay.
14. Select the Channel menu.
15. Change the file name of the symbol table for the C_Ctrl group (or whichever group's symbol table you are replacing) to the one that you specified in step 5.

LABELS

When using 92A96 Modules, you should apply slot number labels to various parts of the modules and DAS 9200 as shown in Figure 3-4. These slot numbers will help you identify which modules are connected to the probe adapter in a multimodule system.

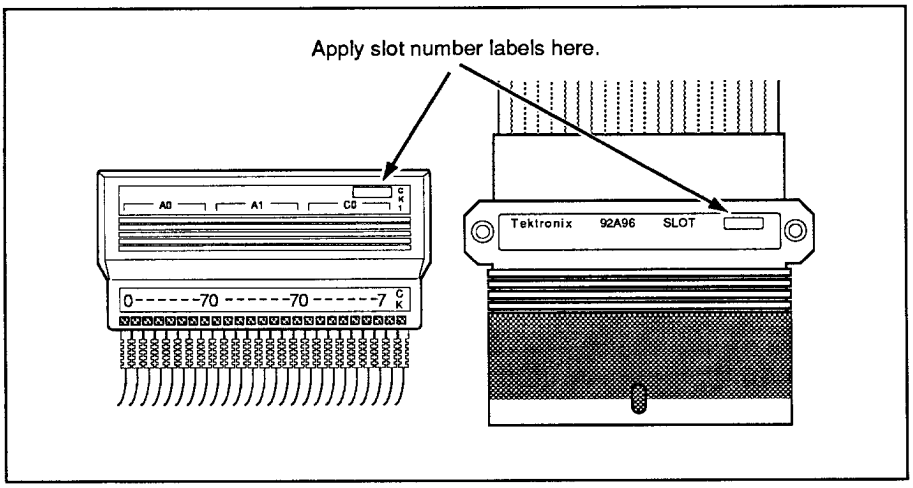


Figure 3-4. Applying slot number labels.

The probe connectors and cables for the 92A96 Module have color-coded labels. Table 3-4 shows the color of the probe connector and cable labels, as well as the module section and clock assignments.

Table 3-4
Label Information

Label Color	Sections	Clock
Orange	A0, A1, C0	Ck 0
Green	A2, A3, C1	Ck 1
Blue	D0, D1, C2	Ck 2
Gray	D2, D3, C3	Ck 3

Individual 8-channel probes are labeled with ground and channel assignments (7–0) only. Ground and channel order identification is marked on the podlet holder. Each channel (podlet) within an 8-channel probe is color-coded, using the standard resistor-value color code, on the signal side of the podlet body to identify its channel number. For example, channel 0 is black and channel 7 is violet as shown in Figure 3-5. Each interface housing connects to three 8-channel probes and a single clock probe.

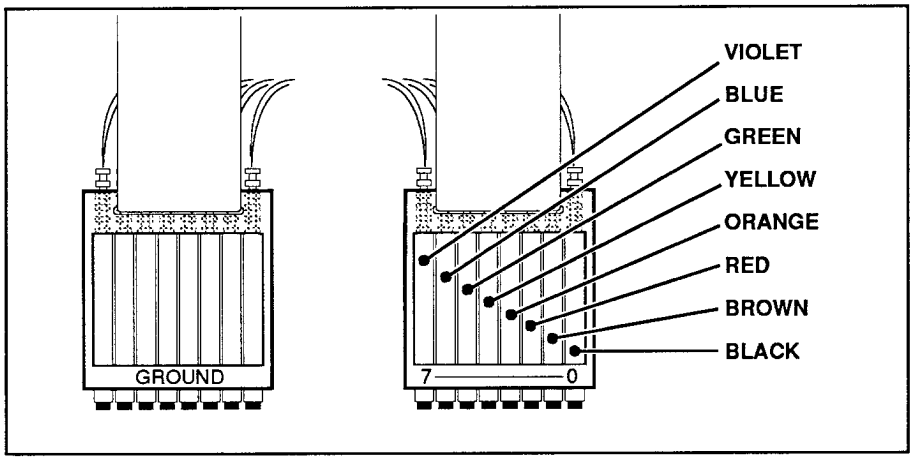


Figure 3-5. Probe channel color and labels on an 8-channel probe.

CONFIGURING THE PROBE ADAPTER

There are two jumpers that you need to configure on the probe adapter. One jumper controls the byte order of acquired data and the other controls the clock used for acquiring disassembly or timing data.

You can move the disassembly/timing jumper whenever you want, but you should configure the probe adapter before placing it in the Am29000/050 system. There may be inadequate space in which to change the position of the disassembly/timing jumper if you place the probe adapter in the Am29000/050 system before configuring it.

Setting the Byte-Order Jumper

The Am29000/050 microprocessor lets you select either Big- or Little-Endian byte ordering for data reads and writes. Big-Endian byte ordering is when the most significant data byte of a multibyte number is located at the lowest address. Little-Endian byte ordering is when the least significant byte of a multibyte number is located at the lowest address.

The byte-order jumper on the probe adapter must be used to set the default byte ordering used for disassembly when you power up the DAS 9200 and Am29000/050. You should set the jumper to match the byte ordering normally used in your Am29000/050 system.

Set the jumper in the B position to acquire data using Big-Endian byte ordering; set it in the L position to acquire data using Little-Endian byte ordering. Setting the jumper to B is the same as initializing bit 2 of the Byte Order (BO) bus for the Am29000/050 configuration register to 0.

Figure 3-6 shows the location of the byte-order jumper on the probe adapter.

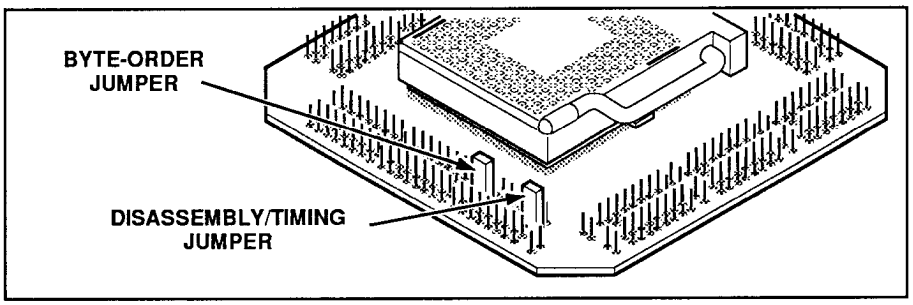


Figure 3-6. Location of the byte-order and disassembly/timing jumpers on the probe adapter.

You can also change the byte order used for disassembly any time between acquisitions in the Data Byte Order field of the Disassembly Format Definition overlay. Refer to the description of the *Disassembly Format Definition Overlay* in Section 4 for details on how to do this.

Setting the Disassembly/Timing Jumper

The disassembly/timing jumper is used in conjunction with clocking selections in the Clock menu. Custom and External clocking sets the 92A96 Module to sample data based on an external clock, in this case, the system clock of the Am29000/050. This type of sampling is commonly called synchronous. Internal clocking sets the 92A96 to sample data based on a clock internal to that module and is commonly called asynchronous.

The jumper must be set in the D position when sampling data synchronously with the Am29000/050 system. Disassembly will only be correct when this jumper is in the D position. You can also view acquired data using Internal clocking (asynchronous) with the jumper in the D position but no data will be seen for the SYSCLK signal. In the D position, the SYSCLK signal, the Am29000/050 system clock signal, is used as a sampling clock source and is not stored as data.

You can set the jumper in the T position when sampling data asynchronously using Internal clocking. The SYSCLK signal is then acquired as data and can be viewed in the display menus.

Figure 3-6 shows the location of the disassembly/timing jumper on the probe adapter.

CONNECTING THE DAS 9200 TO THE Am29000/050 SYSTEM

Before acquiring data you must connect the probe adapter to both the SUT and probe cables of the 92A96 Modules. Your Am29000/050 system must have a minimum amount of clear space surrounding the Am29000/050 microprocessor to accommodate the probe adapter. *Appendix C: Service Information* gives these dimensions.

CAUTION

Static-discharge can damage the Am29000/050 microprocessor, probe adapter, or the 92A96 Modules. To prevent static damage, observe the following precautions while following all the connection procedures.

Handle the microprocessor only in a static-free environment.

Always wear a grounding wrist strap, or similar device, while handling the microprocessor and probe adapter.

This discussion describes how to do the following:

- connect probe cables to interface housings
- configure and place the probe adapter in your SUT
- connect the auxiliary channels on the probe adapter

CONNECTING THE INTERFACE HOUSINGS

The probe cables and interface housings may already be connected. If they are not connected, refer to Figure 3-7 and follow this procedure:

1. Match the color of the label and slot number on the interface housing to the color of the label and slot number on the loose end of a 92A92 probe cable.
2. Line up the key and key slot and connect them.
3. Repeat steps 1 and 2 for the remaining interface housings and probe cables (three for a single module or seven for two modules).

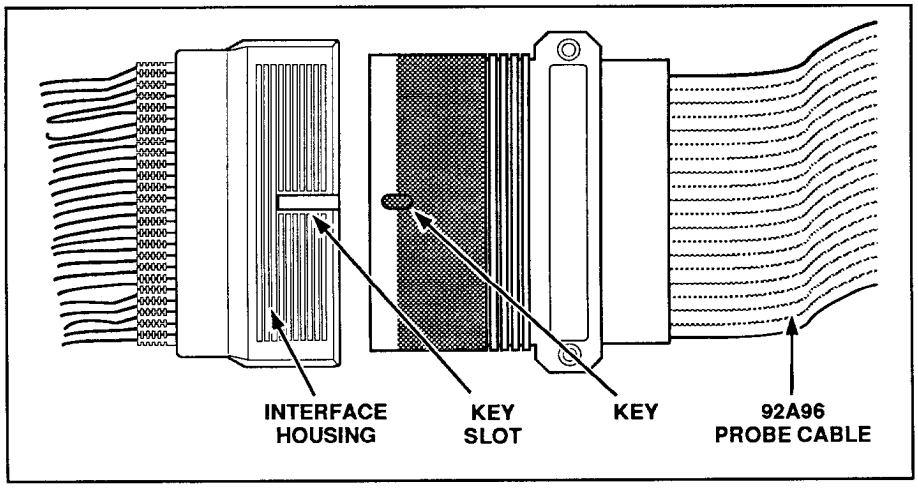


Figure 3-7. Connecting the interface housing to the 92A96 probe cable. The label on the interface housing is not on the side with the key slot.

CONNECTING THE PROBE ADAPTER

Before acquiring data, you must connect the probe adapter to both the clock and 8-channel probes for the 92A96 Module being used, and to the system under test. Your Am29000/050 system must have a minimum amount of clear space surrounding the Am29000/050 microprocessor to accommodate the probe adapter. Figure C-1 in *Appendix C: Service Information* shows these dimensions.

The 92A96 probe cables should already be connected to the 92A96 interface housings. Figures 3-9 and 3-11 show the connections from the 92A96 Module probe cables to the probe adapter.

Connecting the Probes to the Probe Adapter

If you need to regang channels (podlets) within an 8-channel probe together, refer to the discussion on *Replacing 8-Channel Probe Podlets* in Appendix C.

You can connect a single 92A96 Module to acquire data from the code or the data bus only, or two modules to acquire data from both buses. When acquiring data from both buses, the C_Bus module is positioned in the lower-numbered slot and the D_Bus module is positioned in the higher-numbered slot. You should make all the clock and 8-channel probes connections as shown in Figures 3-9 and 3-11 when using two modules.

To connect the clocks and 8-channel probes from the C_Bus module to the probe adapter, follow this procedure:

1. Use the antistatic shipping material to support the probe adapter when connecting the clock and 8-channel probes as shown in Figure 3-8. This prevents the circuit board from being flexed and socket pins on the probe adapter from being bent.

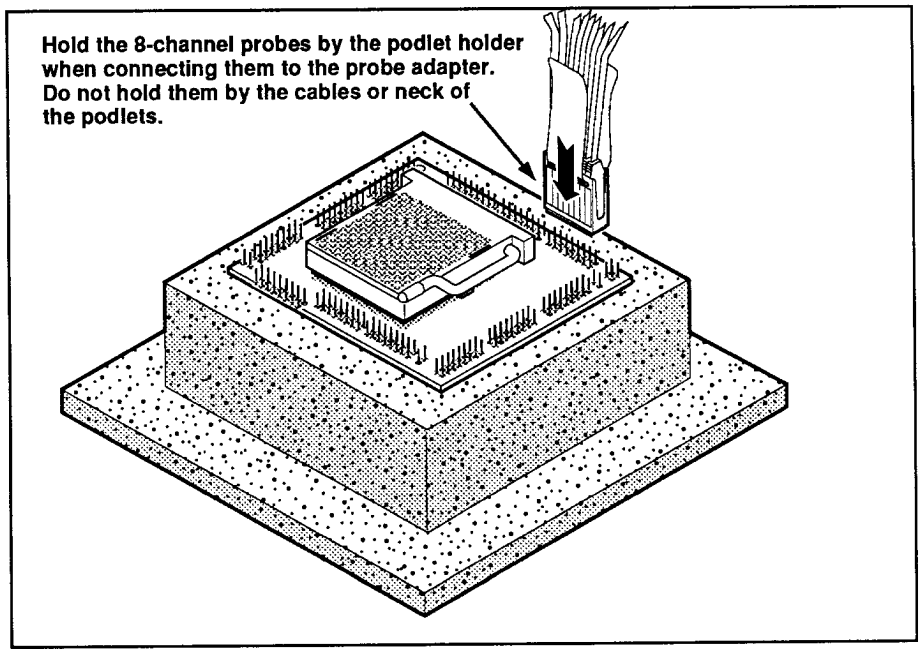


Figure 3-8. Connecting clock and 8-channel probes to the probe adapter.

2. Match the section names and channel numbers on the interface housings to the probe adapter as shown in Figure 3-9. Sections that connect to the code bus have a C- preceding the section name on the probe adapter, such as C-A0, C-A1, and so on. Be sure to match the clock and 8-channel probes from the C_Bus module when using two modules.

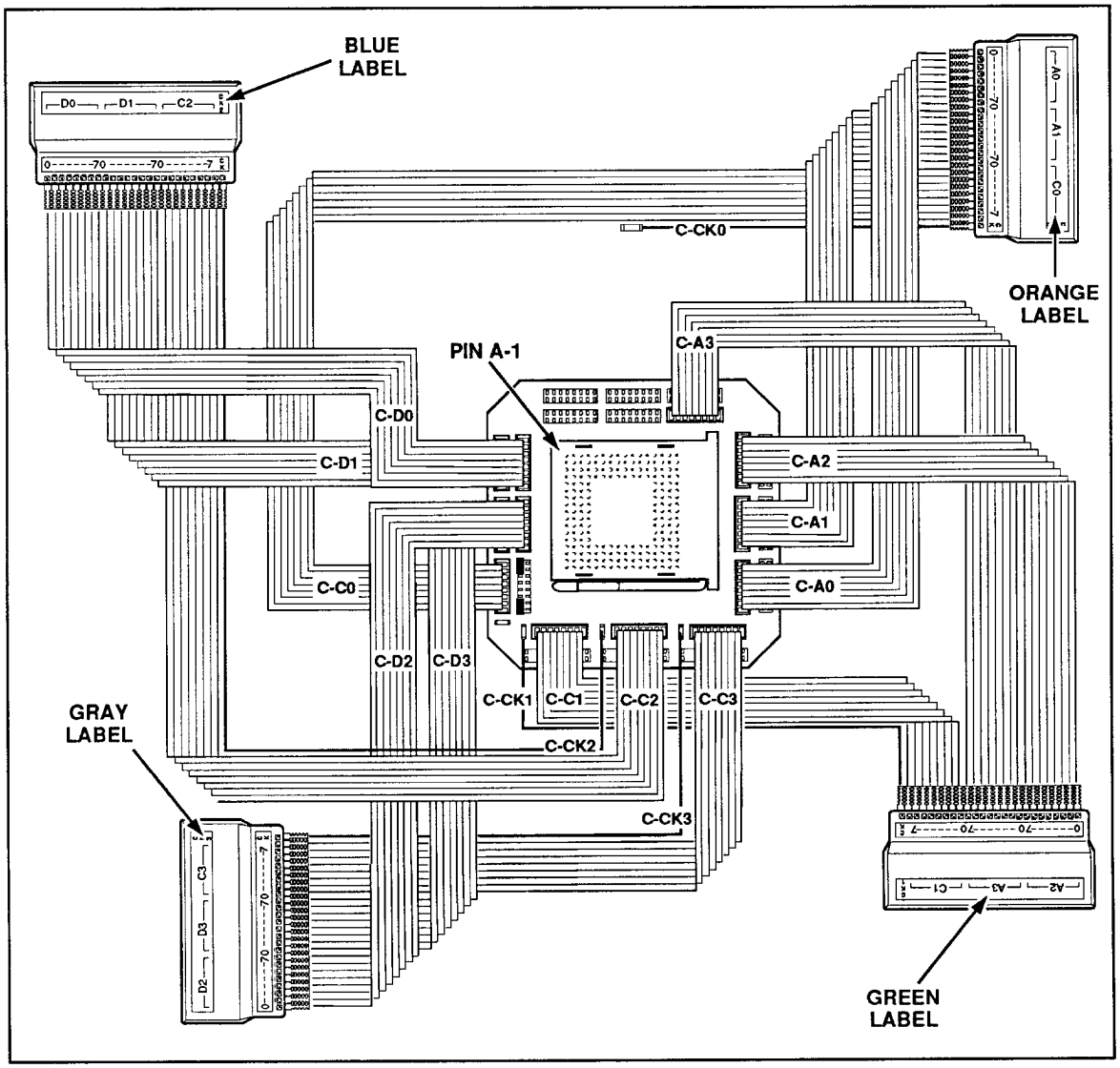


Figure 3-9. Connections from the C_Bus module probes to the probe adapter. Clock 0 of the C_Bus module (C-CK0) does not connect to the probe adapter.

NOTE

Connect the signal connectors to the signal pins and the ground connectors to the ground pins. Connecting any Am29000/050 signal to a probe adapter ground pin can cause the Am29000/050 microprocessor to malfunction.

3. Push each 8-channel probe over the assigned group of square pins as shown in Figure 3-9. Channel numbers printed on the circuit board must match the channel numbers on the 8-channel probes as shown in Figure 3-5.

   If you are connecting four or more adjacent 8-channel probes to the probe adapter, refer to Figure 3-10 and connect the 8-channel probes in the following order:

   a. Connect both 8-channel probes one at a time on the outside groups of square pins on any one side of the probe adapter.
   b. Align and start to connect the center pair of 8-channel probes on the remaining two groups of square pins.
   c. Hold the center two 8-channel probes together as one 16-channel probe and push them onto the square pins.
   d. Align and start to connect the last pair of 8-channel probes on the remaining two groups of square pins.
   e. Hold them together as one 16-channel probe and push them onto the square pins.

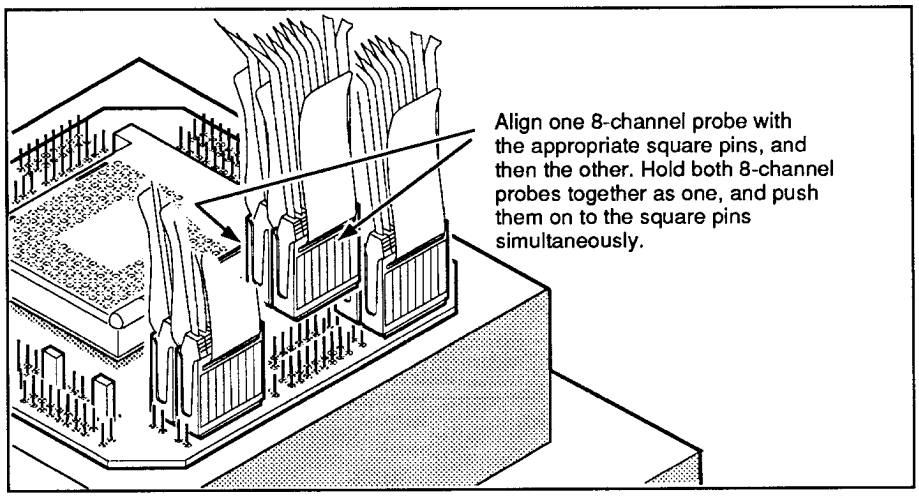


Figure 3-10. Connecting six adjacent 8-channel probes.

4. Line up the label on each clock probe with the appropriate pair of square pins on the probe adapter as shown in Figure 3-9. Be sure to orient the clock probe ground and channel to the ground and clock signal square pins on the probe adapter. The clock pins that connect to the code bus have a C- preceding the clock name on the probe adapter, C-CK1, C-CK2, and C-CK3.

   There are no connections between the clock 0 channel of the C_Bus module and the probe adapter. Therefore, C-CK0 is not shown on the probe adapter.

5. Push each clock probe over the assigned square pins.

NOTE

Be sure to connect the ground channel of the clock probes to the ground square pins (labeled GND) on the probe adapter.

To connect the clocks and 8-channel probes from the D_Bus module to the probe adapter, refer to Figure 3-11 and follow the previous procedure.

Match the section names and channel numbers on the interface housings to the probe adapter. Sections that connect to the data bus have a D- preceding the section name on the probe adapter, such as D-A0, D-A1, and so on. Be sure to match the clock and 8-channel probes from the D_Bus module when using two modules.

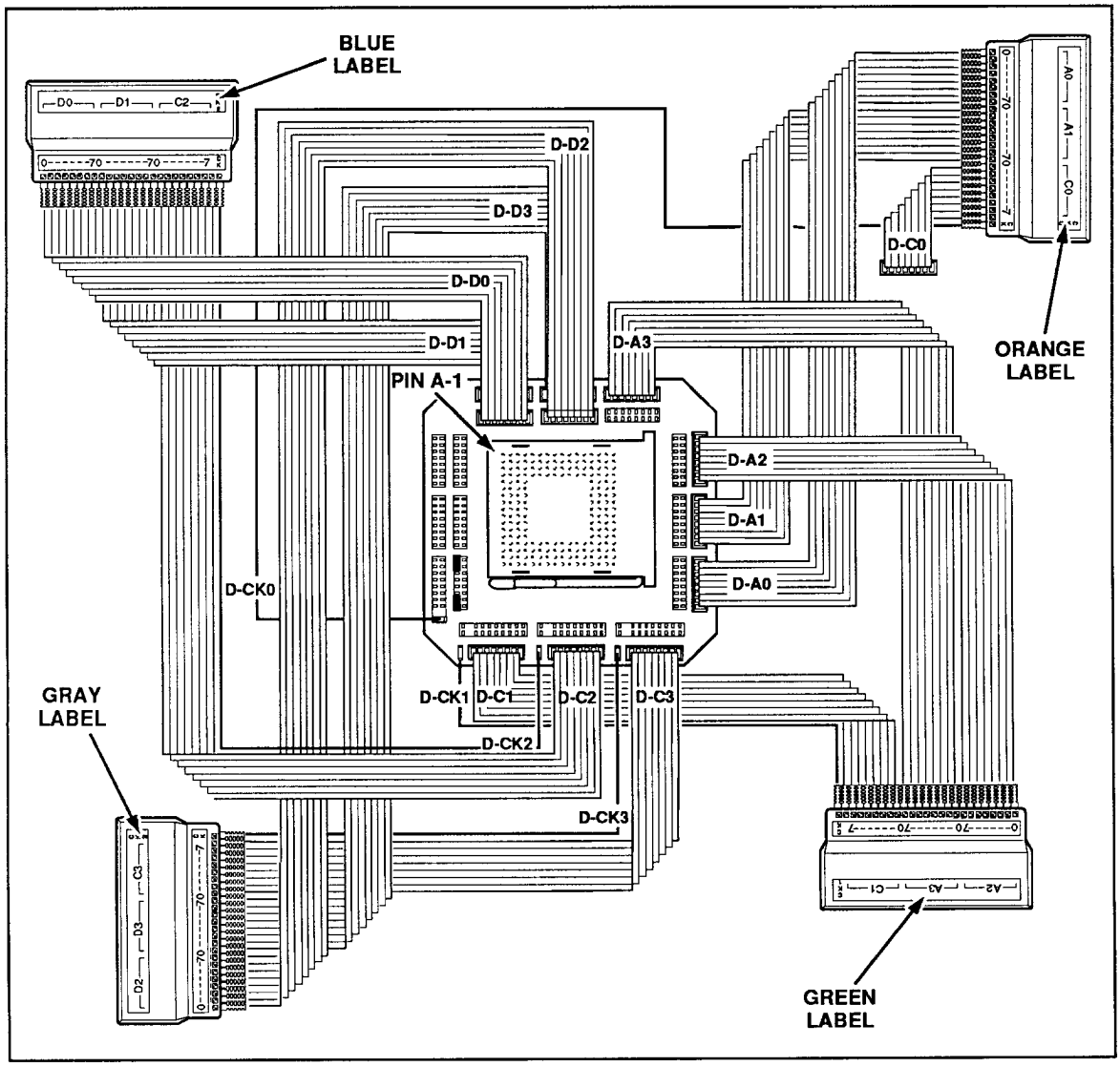


Figure 3-11. Connections from the D_Bus module probes to the probe adapter. Section C0 of the D_Bus module (D-C0) does not connect to the probe adapter.

Placing the Probe Adapter in the SUT

After all the clock and 8-channel probes are connected to the probe adapter, you can place the probe adapter in the Am29000/050 system. To place the probe adapter in the SUT, refer to Figure 3-12 and follow this procedure:

1. Turn off the power to the SUT.

2. Carefully remove the microprocessor from your system.
3. Carefully plug the probe adapter into the Am29000/050 socket of the SUT. Be sure to align pin A-1 of the probe adapter to pin A-1 of the system socket.

CAUTION

You can damage the microprocessor, the sockets on the probe adapter, and the system socket if you do not properly orient the Am29000/050. A-1 is printed on the circuit board. The Am29000/050 has a keying pin, number 169, to ensure proper alignment of pin A-1. Figure 3-11 shows the proper alignment of pin A-1 on the Am29000/050 microprocessor, the ZIF socket, and the Am29000/050 system socket.

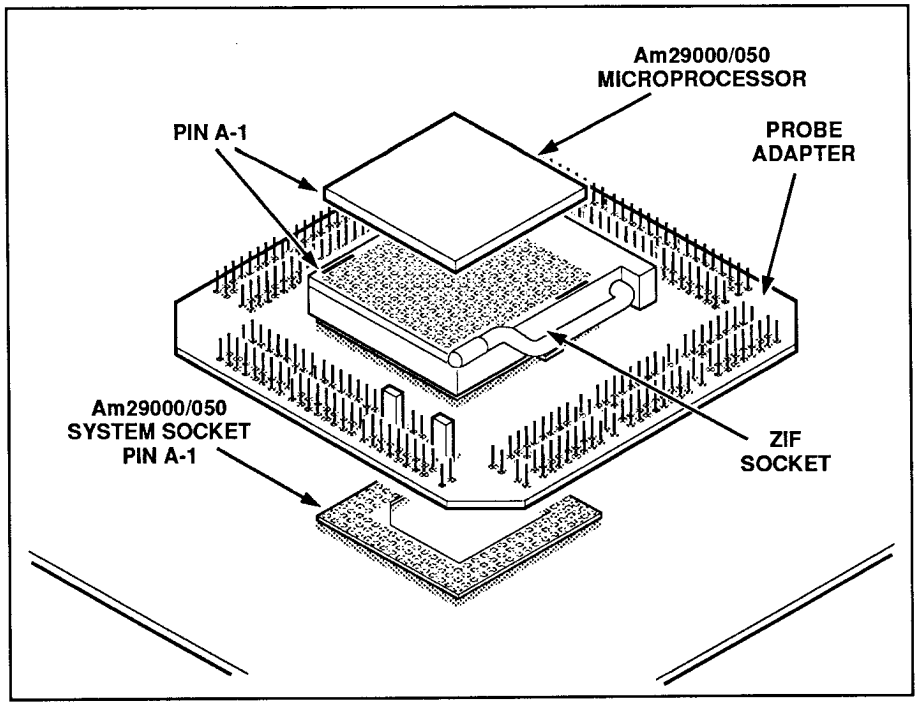


Figure 3-12. Placing the probe adapter in the Am29000/050 system. The clock and 8-channel probes should already be connected before placing the probe adapter in the system. They are not shown connected in this figure because they obscure the detail.

4. Open the ZIF socket on the probe adapter by pulling the lever up and away from the socket.

5. Carefully plug the Am29000/050 microprocessor into the ZIF socket, so that pin A-1 of the microprocessor is inserted into pin A-1 of the ZIF socket.
6. Push the ZIF socket's lever down to lock the ZIF socket in the closed position.

Alternate Connections

If you are acquiring data with two 92A96 Modules, there are 20 individual channels that connect to the Am29000/050 system but are not used for mnemonic disassembly. Some of these signals may be meaningful during disassembly and others are only useful for hardware analysis. These signals and their uses are described in Appendix B.

You can use any of the 20 individual channels and the unused 8-channel probe for section C0 of the D_Bus module for general purpose use to acquire data from other parts of the Am29000/050 system. This brings the total number of channels that you can use to make alternate connections to 28.

Table 3-5 shows the sections and channels you can use to connect to other signals in your Am29000/050 system. The C- sections are from the C_Bus module and the D- sections are from the D_Bus module.

Table 3-5
Channels Available for Alternate Connections

Section	Channels
C-C0	5, 3, 2, 1
C-C1	7
C-C2	6, 5, 4
C-C3	7, 6, 4, 1, 0
D-C0	7, 6, 5, 4, 3, 2, 1, 0
D-C1	6, 5, 1
D-C2	7, 4
D-C3	4, 0

You can use the entire 8-channel probe from section C0 of the D_Bus module, or separate the individual channels (podlets) and connect them to other signals in your Am29000/050 system. You will have to separate the podlets from the sections listed in Table 3-5 to use them for connections to other signals.

Refer to *Disconnecting Clock and 8-Channel Probes* and *Removing and Replacing Podlets* in Appendix C of this manual for information on how to disconnect probes and separate podlets from an 8-channel probe. Also refer to your data acquisition user's manual for information on general purpose applications.

NOTE

Be sure to connect all podlet ground channels to the ground in the Am29000/050 system when making any alternate connections.

You may also need to use a flying leadset (Tektronix part number 012-1353-00) and attach KlipChip adapters (Tektronix part number 020-1386-01) to make alternate connections.

If you want to use these channels for other purposes, you will probably want to change the channel grouping in the Channel menu. To change the default channel grouping, follow these steps:

1. Press the Select Menu key to return to the Menu Selection overlay.
2. Select the Channel menu in the Setup column.
3. Press the Return key.
4. Press F8: ADD. Select Add a Group and press the Return key.
5. The cursor will appear in the Group Name field. You can enter a new group name or use the default group name.
6. Move the cursor to the Section field and enter a section name. Table 3-5 shows the sections and channels you can use to define new groups without disturbing disassembly.
7. Add channels to the new group by entering channel numbers in the Channel field. The DAS 9200 automatically removes channels from existing channel groups as they are used to create new channel groups.
8. After the new groups are defined, press the Select Menu key to exit the Channel menu.

Section 4: ACQUIRING AND VIEWING DISASSEMBLED DATA

The primary function of this product is to assist you during the design period when you try to execute new or untested software on your Am29000/050 hardware. This section describes how to acquire data for viewing in the Disassembly menu.

After you configure the DAS 9200, install the microprocessor support software, make all the connections between the DAS 9200 and the system under test, and select the 29000C or 290000D support or restore the 29000_9696 cluster setup file, you are ready to complete the setup for the C_Bus and D_Bus modules. To complete the setup, you need to choose a clock type and define a trigger program (or use the defaults).

Am29000/050 DISASSEMBLER OPERATION

There are times when the disassembly will be incorrect or will appear to be missing execution cycles. The disassembler cannot always detect which code is fetched and executed and which code is fetched and flushed from the input queue. For instance, the Am29000/050 may take a conditional jump but the disassembler may show that the cycles were executed instead of being flushed.

Figure 4-1 shows an example of such an occurrence. The conditional jump in the example takes the jump, but because the address of the destination of the jump does not cause an address break, the disassembler does not detect it. In addition, none of the acquired Am29000/050 signals can indicate a jump. In this example, there is no direct address for the destination of the jump because the address is in a register.

Cursor: 273 29000C Support

Sequence	C_Addr	C_Data	Mnemonics		Timestamp
266	00800000	00------	(READ)		80 ns
267	00008150	C0000080	JMPI	LR0	190 ns
268	00008154	70400101	NOP		40 ns
269	00008158	70400101	(FLUSH)		40 ns
270	0000815C	70400101	(FLUSH)		40 ns
271	00008044	02808A00	CONSTH	LR10,80000000	80 ns
272	00008048	03808B5C	CONST	LR11,0000805C	40 ns
273	0000804C	CC008A8B	JMPTI	LR10,LR11	40 ns
274	00008050	158A8A01	ADD	LR10,LR10,01	40 ns
275	00008054	158A8A01	ADD	LR10,LR10,01	40 ns
276	00008058	158A8A01	ADD	LR10,LR10,01	40 ns
277	0000805C	C68A0000	MFSR	LR10,VAB	80 ns
278	00008060	02008101	CONSTH	LR1,00010000	40 ns
279	00008064	CE000081	MTSR	VAB,LR1	40 ns
280	00008068	C6810300	MFSR	LR1,CFG	40 ns

Figure 4-1. Example of a conditional jump. Sequences 275 and 276 show the fetched opcodes as executed when they were actually flushed.

You can manually change the erroneously disassembled bus cycle using the F4: MARK DATA key of the Disassembly menu. Figure 4-20 shows this example after it has been corrected using the F4: MARK DATA key. Refer to the description on *Manually Overriding Disassembled Instructions* later in this section for directions on how to do this.

CLOCKING

You can use the Clock menu to set clocking choices to control data sampling. The disassembler software offers a customized-clocking selection for the Am29000/050 microprocessor. This clocking choice (Custom) is used whenever you select the 29000C or 29000D Support in the Configuration menu or restore the 29000_9696 multimodule setup.

The software provides two modes for acquiring Am29000/050 data with the D_Bus module: to include DMA cycles or to exclude DMA cycles. The default is to exclude DMA cycles. You can change the clocking mode by changing the DMA Cycles option field in the Clock menu of the D_Bus module.

The C_Bus module always acquires All Bus Cycles. No options are available for the Clock menu of the C_Bus module.

DMA Cycles. A DMA cycle is defined as the Am29000/050 giving up the bus to an alternate device. This type of cycle is acquired if you select Included for the D_Bus module. This option field lets you choose whether to Include or Exclude DMA cycles.

Figure 4-2 shows the Clock menu for the D_Bus module and the DMA Cycles option field. A description of how DMA cycles are sampled by the disassembler is in Appendix B.

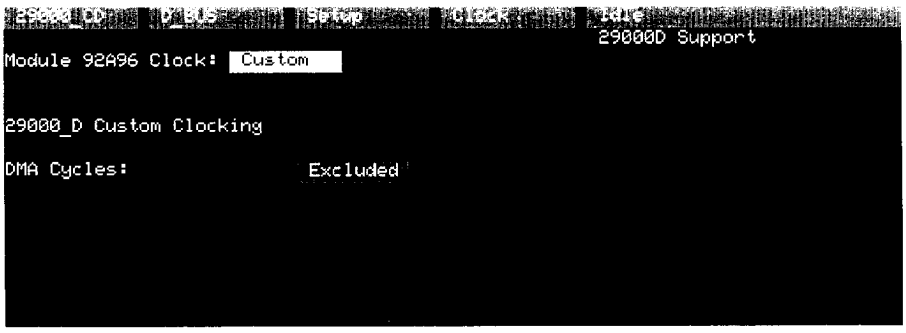


Figure 4-2. Clock menu for the D_Bus module.

Disassembly may not be correct with the Internal or External clocking modes. Refer to the *Hardware Analysis* section for a description of using these other clock selections.

TRIGGERING

The Am29000/050 microprocessor support supplies a default trigger program for the 29000_9696 setup. The default trigger program for a single C_Bus or D_Bus are the same as shown in the module user's manual.

The default multimodule trigger program uses one of the two communication signals dedicated for use with the disassembler. The C-to-D signal is used for communication from the C_Bus module to the D_Bus module. The D-to-C signal is used for communication from the D_Bus module to the C_Bus module.

The multimodule trigger program is set up to search for address bus values that you enter in the word recognizer fields in the Trigger menu of the C_Bus module. When these values are found, the C_Bus module sends the C-to-D signal to the D_Bus module, triggers, and stores data. The trigger program in the Trigger menu of the D_Bus module receives the C-to-D signal from the C_Bus module, triggers, and stores data.

Other Trigger menu selections are available for both modules and are still valid for disassembly. There are, however, certain guidelines that should be followed when defining an Am29000/050 trigger program using two modules.

1. Whenever a state uses a trigger action, the appropriate communication signal should be sent as an action to the other module.
2. Whenever one of the communication signals is sent, each state in the trigger program of the other module should be set up to receive that signal.
3. Modules should be clustered together to have a common start signal.
4. The clocking should match between modules for most applications.

Figure 4-3 shows the default trigger program for the C_Bus module with the 29000_9696 multimodule setup file.

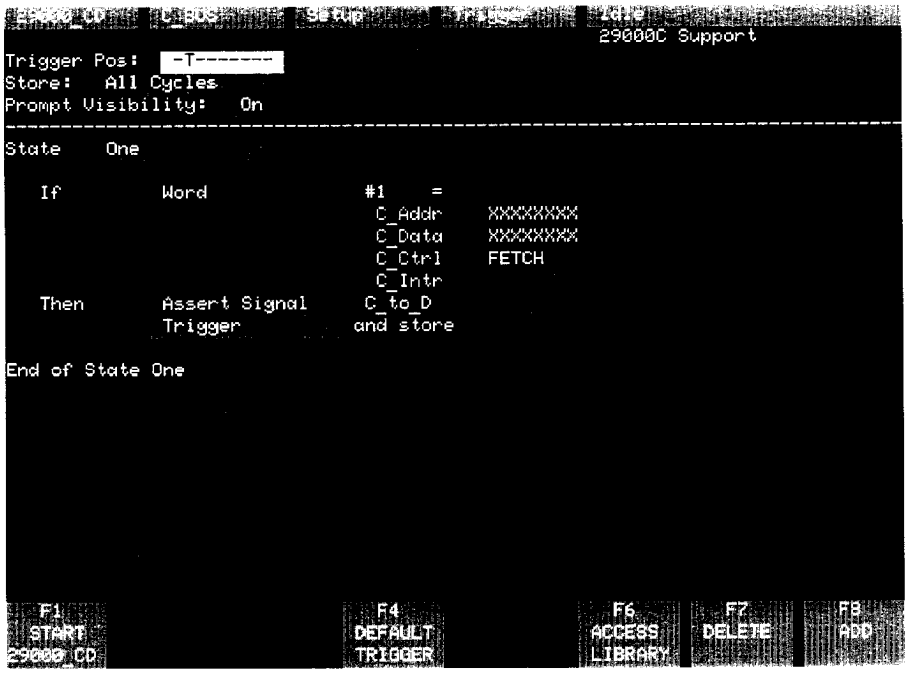


Figure 4-3. Trigger program default setup for the C_Bus module. This trigger program is for the 29000_9696 setup.

Figure 4-4 shows the default trigger program for the D_Bus module with the 29000_9696 multimodule setup file.

Figure 4-4. Trigger program default setup for the D_Bus module. This trigger program is also for the 29000_9696 setup.

ACQUIRING DATA

After you set up the disassembler to acquire data from your Am29000/050 system, you can press F1: START to begin the acquisition. After satisfying the trigger program and filling acquisition memory, the DAS 9200 displays data in the format used last. You may need to press F1: STOP if the stop conditions are not met. The default display format is State. You can change the display format from the Menu Selection overlay (press the Select Menu key).

If the trigger is not located immediately, the DAS 9200 displays the Module Monitor menu showing the progress of the acquisition. Refer to the *Error Messages and Disassembly Problems* appendix for a list of error messages and possible solutions.

DISPLAYING DISASSEMBLED DATA

The DAS 9200 displays disassembled data in the Disassembly menu. This menu shows the disassembled bus cycles, instruction mnemonics, operands and addresses, and data values.

You can display the disassembled data in different formats. You can select the display format and tailor it for your specific needs using the Disassembly Format Definition overlay. Detailed information on this overlay is provided later in this section.

Display Formats

The AM29000/050 disassembler software provides four formats for displaying disassembled data:

- Hardware format shows all acquired cycle types and instruction mnemonics in the order they occurred
- Software format suppresses all opcode extensions and flushed cycles and displays a menu that looks similar to an assembly language program listing
- Control Flow format only displays the instructions that change the control flow of the microprocessor
- Subroutine format only displays subroutine calls, and interrupt/trap calls and returns

You can further define how the data is displayed within the four formats by selecting various display options with the Disassembly Format Definition overlay. For example, to disassemble data from an Am29050 microprocessor, select 29050 in the Processor Choice field.

Figure 4-5 shows an example of the Disassembly menu.

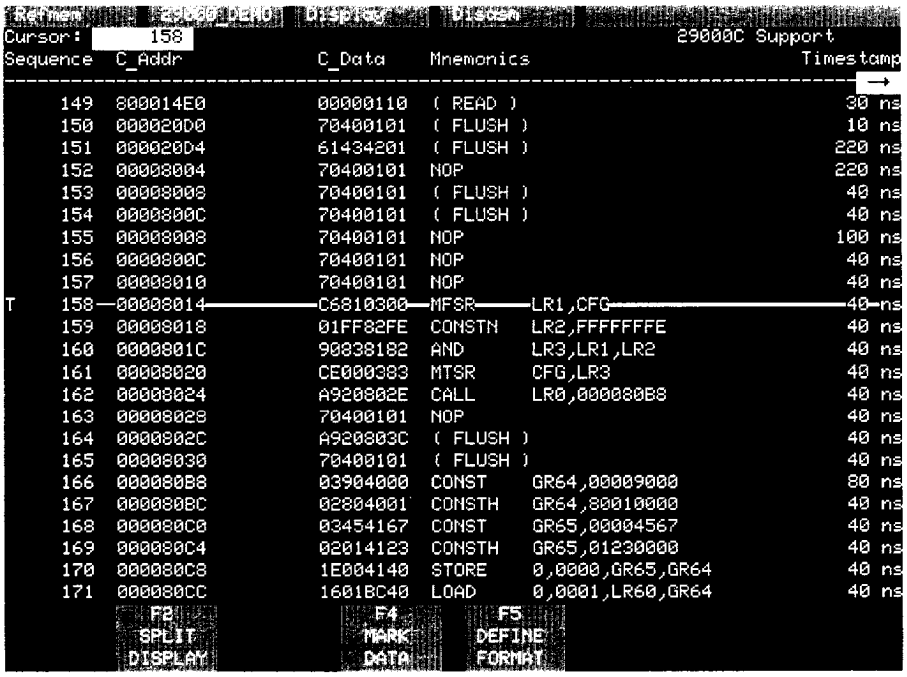


Figure 4-5. Disassembly menu.

No matter which display format you decide to use, the disassembler software displays information in the Disassembly menu in the following columns:

- **Sequence Column.** The sequence column shows the sequence number of the data displayed on that line. The cursor field in the upper-left area of the menu displays the sequence number of the current cursor location.

- **C_Addr or D_Addr Group Columns.** The C_Addr or D_Addr group column shows values for the address portion of the C_Bus or D_Bus module at each sequence. You can display the C_Addr or D_Addr group either symbolically or as an eight-digit hexadecimal value.

- **C_Data or D_Data Group Columns.** The C_Data or D_Data group column shows values for the data portion of the C_Bus or D_Bus module at each sequence. The D_Data group is always displayed as an eight-digit hexadecimal value unless you select Off for the radix. To display the C_Addr or D_Addr groups symbolically, refer to *Displaying the C_Addr and D_Addr Groups Symbolically* in this section.

- **Mnemonics Group Column.** The instruction mnemonics column shows the disassembled Am29000/050 cycles and instructions. When 29000 is selected in the Processor Choice field of the Disassembly Format Definition overlay, the disassembler software displays disassembled instructions and operands as they are described in the *Am29000 32-Bit Streamlined Instruction Processor User's Manual* (1988). When 29050 is selected in the Processor Choice field, the disassembler software displays disassembled instructions and operands as they are described in the *Am29050 Microprocessor User's Manual* (1991).

  The disassembler displays all numeric operands as hexadecimal values. Register numbers are in decimal. When you select the Symbol radix for the C_Addr and D_Addr group, the calculated effective addresses are displayed symbolically.

  If the addressing mode is IP-with-displacement (instruction pointer plus displacement), the disassembler software calculates the effective address before displaying it (instead of displaying the displacement).

- **Timestamp Column.** The timestamp column shows the timestamp value, when you choose to display the timestamp values. You can use the Timestamp field of the Disassembly Format Definition overlay to select Absolute, Relative, Delta, or Off.

  Timestamp values show the amount of time that has elapsed between data samples. There are three ways to show the timestamp value in the Disassembly menu: Absolute, Relative, and Delta. An Absolute timestamp shows the amount of time elapsed immediately after pressing F1: START and each subsequent sample. A Relative timestamp shows the amount of time elapsed between successive samples. A Delta timestamp shows the amount of time elapsed between the data sample you mark with a delta and each previous and subsequent sample. (To place a delta mark on a sample, use F4: MARK DATA from the Disassembly menu.) If there is no delta mark and you select Delta timestamp, then the first data sample (sequence 0) is used as the default delta mark.

Cycles are assigned the value of the timestamp counter at the time that the 92A96 master clock occurs. Because the timestamp counter changes in 10 ns increments, timestamps for data acquired from an Am29000/050 system with a clock rate that is not synchronous with the timestamp counter will be slightly skewed. For example, data acquired from an Am29000/050 system with a clock rate of 30 MHz (33 ns) would be assigned a relative timestamp either of 30 or 40 ns. This skewing is not cumulative.

Keep in mind the following characteristics of the Disassembly menu when viewing disassembled data:

- as you scroll through data, the group names will change to reflect the module's group names from which data was acquired
- all numeric values are shown unsigned (non-negative numbers) except for some relative timestamp values
- all numeric values are justified from the least significant bit
- the timestamp value is always displayed as a decimal value
- the timestamp for all the modules in a cluster is shown only in a single column position
- the only radix selections for Mnemonics are ASCII or Off
- you can only select the Symbol radix when a symbol table is available for that group

The following discussions describe the four display formats.

Hardware Display Format

In the Hardware format, all acquired bus cycles are shown in the order they occurred. Instruction mnemonics are displayed on instruction Fetch cycles and cycle-type information is displayed for all other cycles. Non-instruction bus cycles are displayed as 32-bit wide data transactions. Invalid data bytes are represented by dashes. Figure 4-6 shows the Hardware display format for the Am29000 microprocessor.

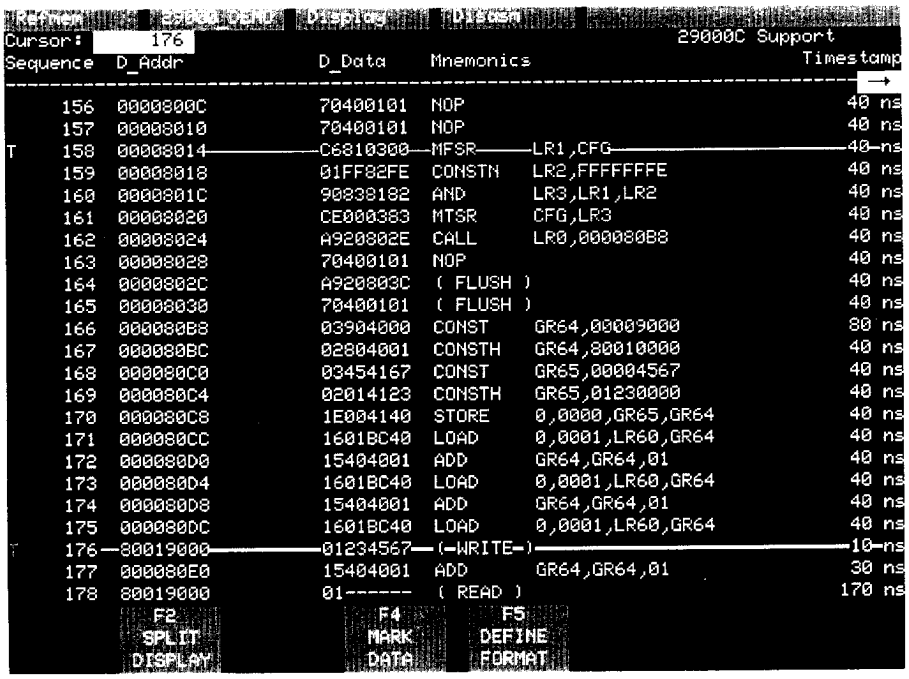


Figure 4-6. Hardware display format for the Am29000.

Figure 4-7 shows the Hardware display format for the Am29050 microprocessor. There are eight more instructions for the Am29050 than for the Am29000. Some of the additional Am29050 instructions are shown in this figure.

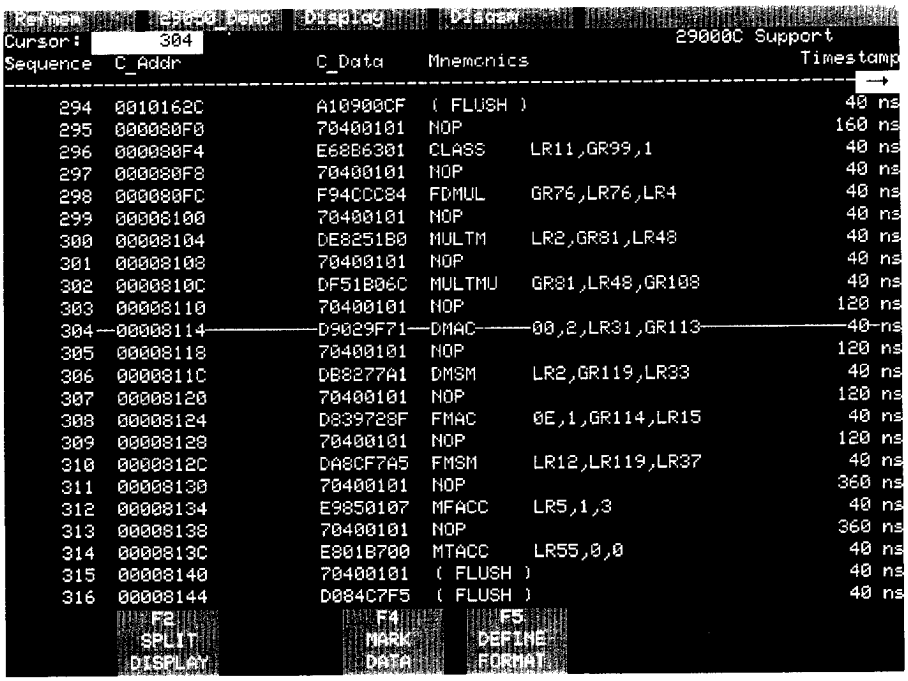


Figure 4-7. Hardware display format for the Am29050.

Software Display Format

In the Software format, only instruction fetches are displayed. All other cycle types are suppressed such as data reads, data writes, and flushed instructions. Figure 4-8 shows the Software display format.

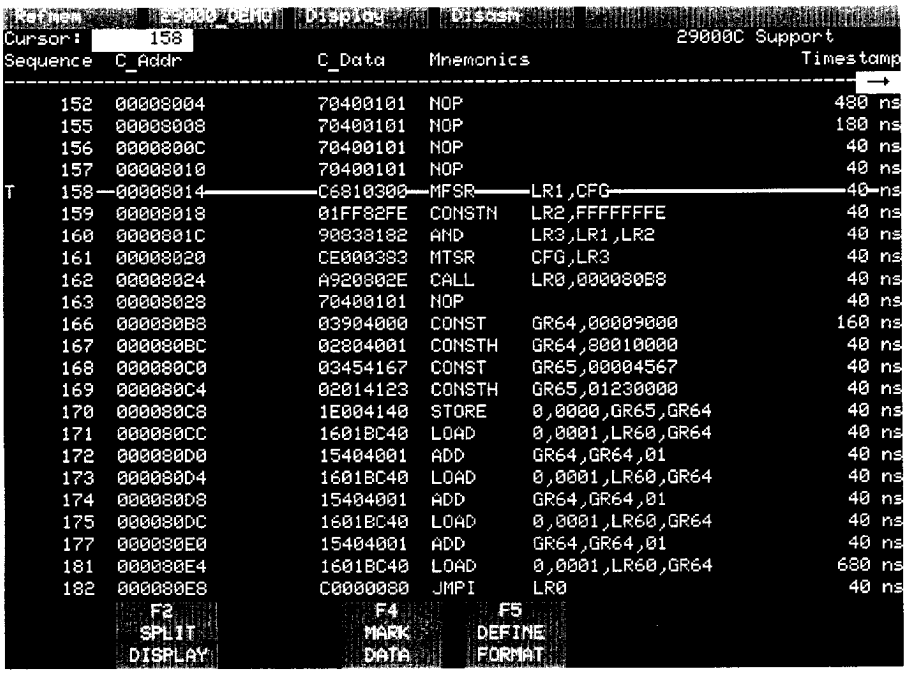


Figure 4-8. Software display format.

Control Flow Display Format

In the Control Flow format, only instructions that change the control flow are displayed. Instructions that do not actually change the control flow are not displayed, such as a conditional branch that is not taken.

Instructions that generate a change in the flow of control in an Am29000 microprocessor are as follows:

CALL	DGT	FDMUL	JMP
CALLI	DIVIDE	FEQ	JMPI
CLASS	DIVIDU	FGE	MULTIPLU
CONVERT	DMUL	FGT	MULTIPLY
DADD	DSUB	FMUL	MULTM
DDIV	EMULATE	FSUB	MULTMU
DEQ	FADD	IRET	SQRT
DGE	FDIV	IRETINV	

Instructions that generate a change in the flow of control in an Am29050 microprocessor are as follows:

CALL	DIVIDE	IRET	JMPI
CALLI	DIVIDU	IRETINV	MULTM
CONVERT	EMULATE	JMP	SQRT

Instructions that can generate a change in the flow of control based on a condition or setting in the control register in an Am29000/050 microprocessor are as follows:

ASEQ	ASLE	ASNEQ	JMPFDEC
ASGE	ASLEU	HALT	JMPFI
ASGEU	ASLT	INV	JMPT
ASGT	ASLTU	JMPF	JMPTI
ASGTU			

Figure 4-9 shows the Control Flow display format.

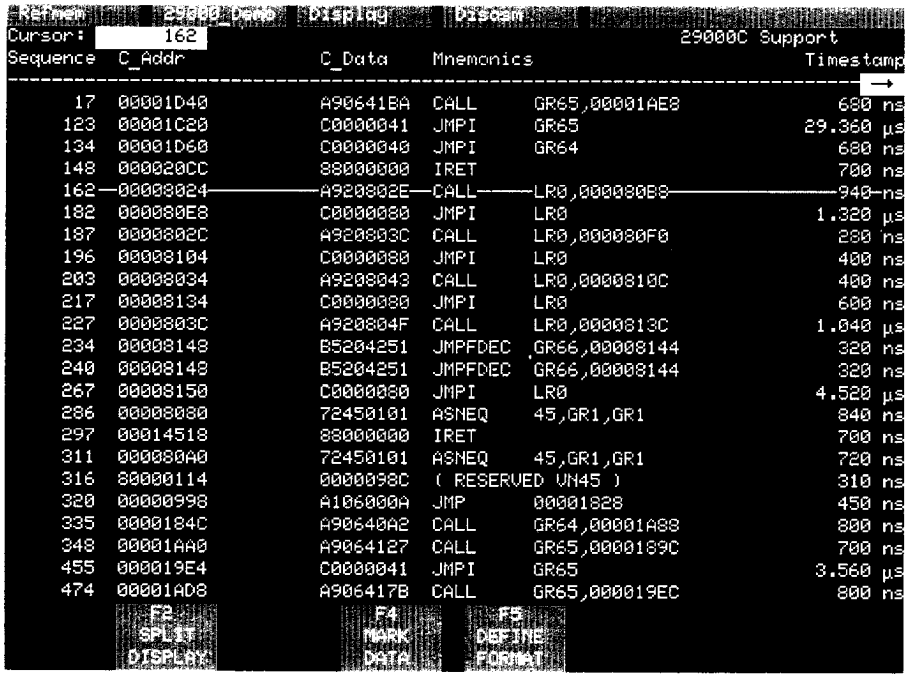


Figure 4-9. Control Flow display format.

Subroutine Display Format

The Subroutine format displays subroutine calls, and interrupt/trap calls and returns only.

Instructions that generate a subroutine call or an interrupt/trap return in an Am29000 microprocessor are as follows:

CALL	DGE	FADD	FSUB
CALLI	DGT	FDIV	IRET
CLASS	DIVIDE	FDMUL	IRETINV
CONVERT	DIVIDEV	FEQ	MULTIPLU
DADD	DMUL	FGE	MULTIPLY
DDIV	DSUB	FGT	
DEQ	EMULATE	FMUL	

Instructions that generate a subroutine call or an interrupt/trap return in an Am29050 microprocessor are as follows:

CALL	CONVERT	DIVIDEV	IRET
CALLI	DIVIDE	EMULATE	IRETINV

Figure 4-10 shows the Subroutine display format.

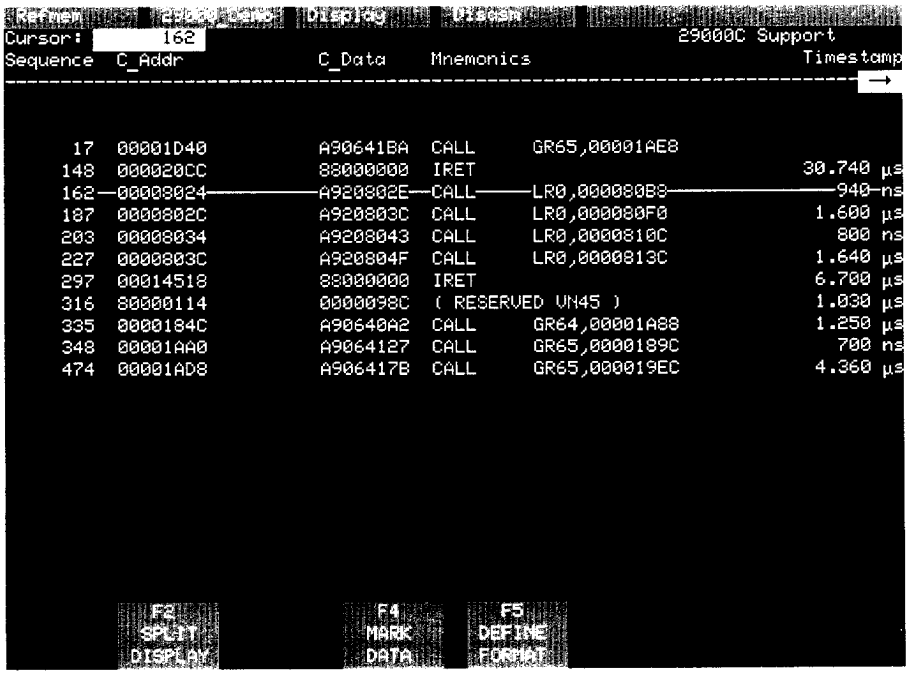


Figure 4-10. Subroutine display format.

Disassembly Format Definition Overlay

The Disassembly Format Definition overlay allows you to tailor the Disassembly menu. To access this overlay, press F5: DEFINE FORMAT from the Disassembly menu.

You can use this overlay to do the following:

- choose the format (mode) in which the Disassembly menu displays disassembled data
- choose disassembly for an Am29000 or Am29050
- set the interval in which the data cursor will scroll through disassembled data
- display and define the format of the timestamp
- highlight various types of disassembled cycles or gaps
- continue disassembly across gaps in the acquisition
- change the order in which the channel groups are displayed in the Disassembly menu
- change the radix for each group
- choose which symbol table to use for each group where symbolic is the selected radix

Figure 4-11 shows the Disassembly Format Definition overlay.

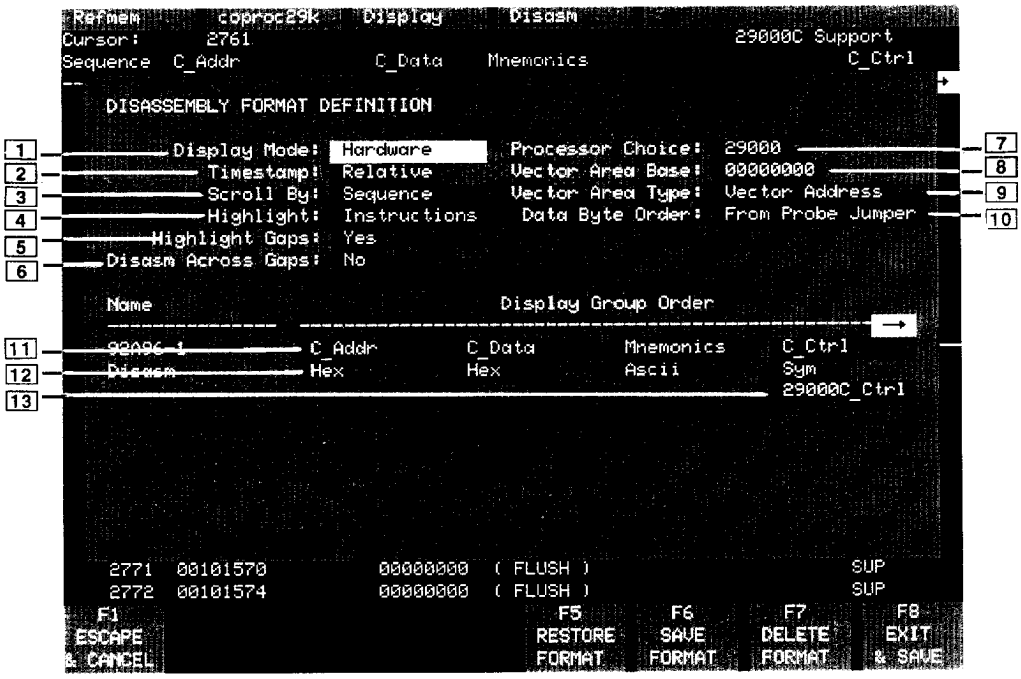


Figure 4-11. Disassembly Format Definition overlay.

[1] **Display Mode.** You can display the disassembled cycle types or instruction mnemonics in Hardware, Software, Control Flow, or Subroutine modes.

[2] **Timestamp.** You can display the timestamp as an Absolute, Relative, or Delta value. You can also set the timestamp display to Off. Refer to the description of timestamp column earlier in this section for definitions of these selections.

[3] **Scroll By.** You can scroll by Sequence, Instructions, Control Flow, or Subroutines.

[4] **Highlight.** You can highlight All, Instructions, Control Flow, or Subroutines. Only the selected type of samples are shown as white text with a black background with highlighting on. All other samples are shown as gray text with a black background.

[5] **Highlight Gaps.** You can choose to highlight or not to highlight gaps. Gaps are caused by qualifying data storage in the Trigger menu and are indicated by a gray background behind the address values.

[6] **Disasm Across Gaps.** You can choose to continue or to discontinue to disassemble instructions across gaps. Disassembling instructions across gaps causes the disassembler to align the last address or data sample before the gap with the address or data sample immediately following the gap. Disassembled data will be invalid if these samples do not logically match.

[7] **Processor Choice.** You can disassemble data according to Am29000 or Am29050 instructions described in the *Am29050 Streamlined Instruction Microprocessor Advance Information Manual* (1990) and the *Am29050 Microprocessor User's Manual* (1991).

[8] **Vector Area Base.** You must enter the full base address for the vector, not the vector address value placed in the Vector Area Base register 0. The default vector area base value is 0. Refer to the *Am29000 32-Bit Streamlined Instruction Processor User's Manual* (1988) or the *Am29050 Microprocessor User's Manual* (1991) for information about vector areas.

[9] **Vector Area Type.** You can choose the type of vector address to display as Vector Address or Instruction Block. Refer to the *Am29000 32-Bit Streamlined Instruction Processor User's Manual* (1988) or the *Am29050 Microprocessor User's Manual* (1991) for information about vector area types.

10 **Data Byte Order.** You can change the byte order in which data is displayed. The byte order choices are Set by Probe Jumper, Big-Endian, Little-Endian, or Display Full Word. Refer to the *Am29000 32-Bit Streamlined Instruction Processor User's Manual* (1988) or the *Am29050 Microprocessor User's Manual* (1991) for information about data byte order.

11 **Group Name.** You can specify the name of the group that displays in the column in which the cursor is positioned. When you move a group, the group is inserted in the new column position and removed from its old position. All the groups to the right of the inserted group are moved over one column position to the right.

12 **Group Radix.** You can select the radix in which each group displays. The radix selections for most groups are Binary, Octal, Hexadecimal, Symbol, and Off. The only selections for the Data group are Hexadecimal or Off. The only selections for Mnemonics are ASCII or Off. You should only select the Symbol radix when a symbol table is available for that group. The timestamp value always displays in decimal.

13 **Symbol Table.** You can specify a symbol table to use for each group where symbolic is the selected radix.

Function Keys

F1: ESCAPE & CANCEL. Closes the overlay and discards any changes you have made since entering it.

F5: RESTORE FORMAT. Displays a list of saved disassembly formats. Use the cursor keys to select the desired format to restore and press the Open/Close or Return key.

F6: SAVE FORMAT. Saves the current selections for the Disassembly Format Definition overlay in a file on disk. You can enter a file name up to ten characters long.

F7: DELETE FORMAT. Displays a list of saved disassembly format files for the current module or cluster setup. Use the cursor keys to select the desired format to delete and press the Open/Close key. You cannot delete the Default format.

F8: EXIT & SAVE. Exits the overlay and executes or saves any changes made.

Bus Cycle Types

Bus cycles are displayed according to the *Am29000/050 System Requirements and Restrictions* described in Section 1 of this manual.

Table 4-1 describes the bus cycle types that the disassembler displays when viewing data in the Hardware format.

Table 4-1
92DM72A Bus Cycle Types

Cycle Type	Description
READ	A cycle in which a read from memory occurs
WRITE	A cycle in which a write to memory occurs
INPUT	A cycle in which a read from an I/O device occurs
OUTPUT	A cycle in which a write to an I/O device occurs
DMA _CYCLE	A cycle in which another master controls the bus
FLUSH*	A cycle in which an instruction fetch is not executed by the microprocessor

*These cycles are calculated or predicted by the disassembler. They cannot be used for triggering in the 92A96 Trigger menu and they are not displayed in the State menu.

Figures 4-12 and 4-13 shows how disassembled READ, WRITE, and FLUSH cycles are displayed by the DAS 9200. Only a portion of the Disassembly menu is shown in each figure. INPUT, OUTPUT, and DMA_CYCLE cycles look similar to READ and WRITE cycles. Examples of these cycles are not shown because they did not occur on the system from which the reference memory data was acquired. Refer to *Appendix B: How Data is Acquired* to see when the various signals used to disassemble data are sampled.

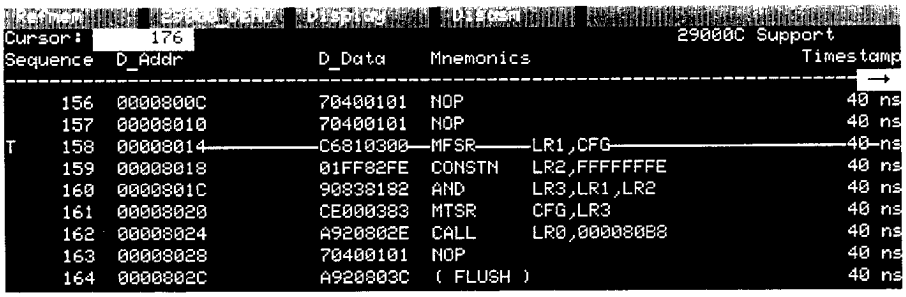
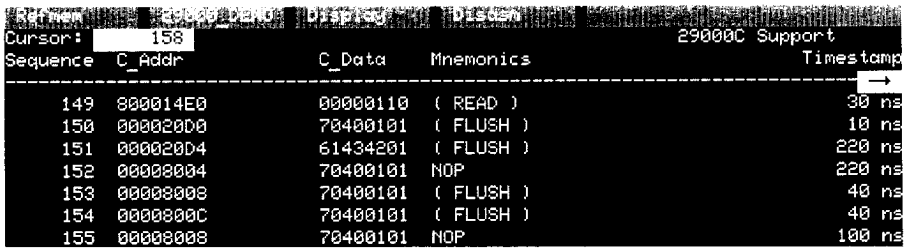


Figure 4-12. Displayed READ and WRITE cycles.



Cursor: 158 29000C Support

Sequence	C_Addr	C_Data	Mnemonics	Timestamp
149	800014E0	00000110	(READ)	30 ns
150	000020D0	70400101	(FLUSH)	10 ns
151	000020D4	61434201	(FLUSH)	220 ns
152	00008004	70400101	NOP	220 ns
153	00008008	70400101	(FLUSH)	40 ns
154	0000800C	70400101	(FLUSH)	40 ns
155	00008008	70400101	NOP	100 ns

Figure 4-13. Displayed FLUSH cycles.

Byte Ordering

You can select either Big- or Little-Endian byte ordering for data reads and writes. Big-Endian byte ordering is when the most significant data byte of a multibyte number is located at the lowest address. Little-Endian byte ordering is when the least significant byte of a multibyte number is located at the lowest address. The byte ordering should match between the Am29000/050 and disassembler for correct disassembly.

Fetches are always full-word accesses for the C_Bus module.

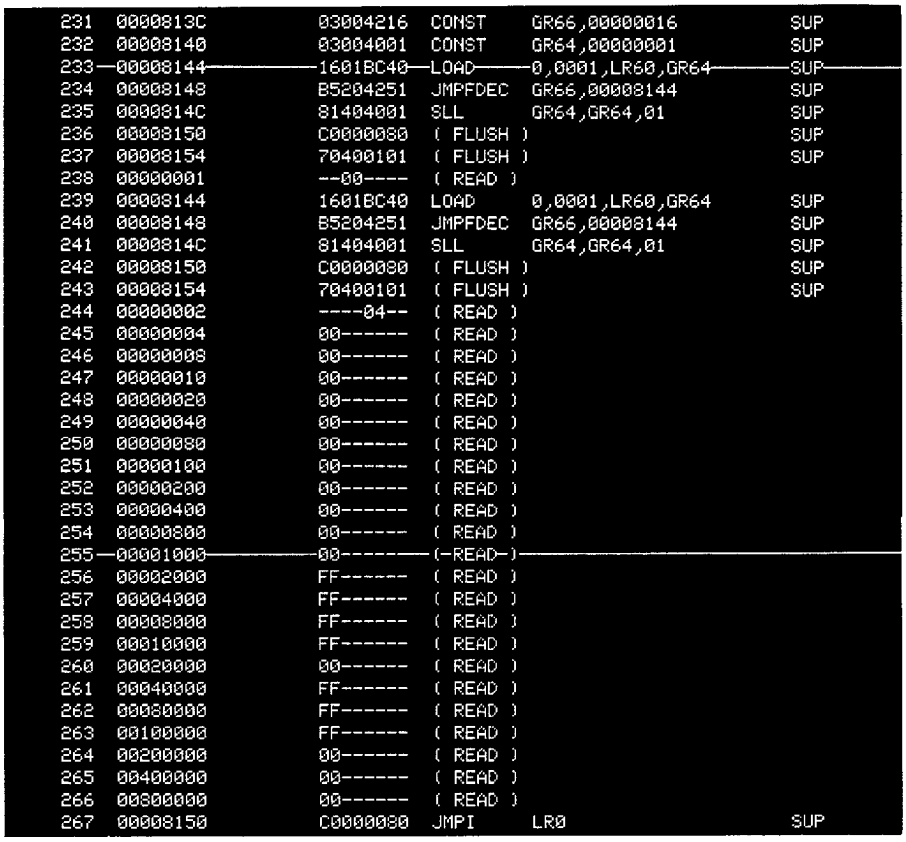
Branch Target Cache

The Branch Target Cache is internal to the Am29000/050 and is inaccessible to the DAS 9200.

When the Branch Target Cache is enabled, the first time a memory location is branched to, the first four instructions are visible to the DAS 9200 and are acquired and displayed. During subsequent branches to that same memory location, the first four instructions at that address will not be visible because they are taken from this cache. Therefore, the first four instructions will be missing from the disassembled data each time that the Branch Target Cache is used.

When you disable the Branch Target Cache, instructions are visible allowing the DAS 9200 to acquire and display them.

Figure 4-14 shows an example of data acquired with the Branch Target Cache enabled. This figure shows more than one screenful of sequences.



```
231  0000813C          03004216  CONST    GR66,00000016          SUP
232  00008140          03004001  CONST    GR64,00000001          SUP
233  00008144          1601BC40  LOAD     0,0001,LR60,GR64       SUP
234  00008148          B5204251  JMPFDEC  GR66,00008144          SUP
235  0000814C          81404001  SLL      GR64,GR64,01           SUP
236  00008150          C0000080  ( FLUSH )                       SUP
237  00008154          70400101  ( FLUSH )                       SUP
238  00000001          --00----  ( READ )
239  00008144          1601BC40  LOAD     0,0001,LR60,GR64       SUP
240  00008148          B5204251  JMPFDEC  GR66,00008144          SUP
241  0000814C          81404001  SLL      GR64,GR64,01           SUP
242  00008150          C0000080  ( FLUSH )                       SUP
243  00008154          70400101  ( FLUSH )                       SUP
244  00000002          ----04--  ( READ )
245  00000004          00------  ( READ )
246  00000008          00------  ( READ )
247  00000010          00------  ( READ )
248  00000020          00------  ( READ )
249  00000040          00------  ( READ )
250  00000080          00------  ( READ )
251  00000100          00------  ( READ )
252  00000200          00------  ( READ )
253  00000400          00------  ( READ )
254  00000800          00------  ( READ )
255  00001000          00------  (-READ-)
256  00002000          FF------  ( READ )
257  00004000          FF------  ( READ )
258  00008000          FF------  ( READ )
259  00010000          FF------  ( READ )
260  00020000          00------  ( READ )
261  00040000          FF------  ( READ )
262  00080000          FF------  ( READ )
263  00100000          FF------  ( READ )
264  00200000          00------  ( READ )
265  00400000          00------  ( READ )
266  00800000          00------  ( READ )
267  00008150          C0000080  JMPI     LR0                    SUP
```

Figure 4-14. Acquired data with the Branch Target Cache enabled.

In Figure 4-14, sequence 231 shows a loop counter being initialized for a loop where byte accesses are performed by shifting the address. This method could be used to test the address lines for shorts.

Sequence 232 is the initial address. Sequence 233 is the first instruction in the loop and reads a byte from the address in Global Register 64. Sequence 234 tests for the end of the loop. It is this instruction that causes the cache to turn on. Sequence 235 is executed because it is the delayed slot. This also shifts the address bit for the Load instruction. Sequence 238 is the result of the load in sequence 233. Addresses 8144, 8148, and 814C are re-executed. Instructions are also stored into the cache. Starting with the third time through the loop, the execution unit is executing completely from the Branch Target Cache. Sequences 245 through 266 result from the Load instruction of the loop. Sequence 267 is the first cycle out of the loop after the test of the loop failed.

Burst Mode and Address Signals, A0 – A11

The probe adapter latches the initial address of a Burst cycle for address lines A0 through A11. Circuitry on the probe adapter then increments the address each time the Instruction Ready signal is asserted until the Burst is finished.

The disassembler always displays the logical address. The address is latched and incremented only for the C_Bus module.

You can use data from any part of the Burst cycle as a word recognizer value in your trigger program (Trigger menu) for the C_Bus module.

NOP Opcode

The NOP mnemonic is a no operation opcode that does not appear in the manual for the Am29000. There are certain operations that require a NOP opcode. The disassembler recognizes the following instruction as a NOP:

```
ASEQ    0x40, GR1, GR1
```

Floating Point Instructions

The display of Am29000 and Am29050 floating point instructions are different. The Am29050 microprocessor contains an internal floating point unit. The Am29000 microprocessor requires an external device for floating point calculations.

Figure 4-15 shows the how floating point instructions appear for the Am29000. Figure 4-16 shows the how floating point instructions appear for the Am29050.

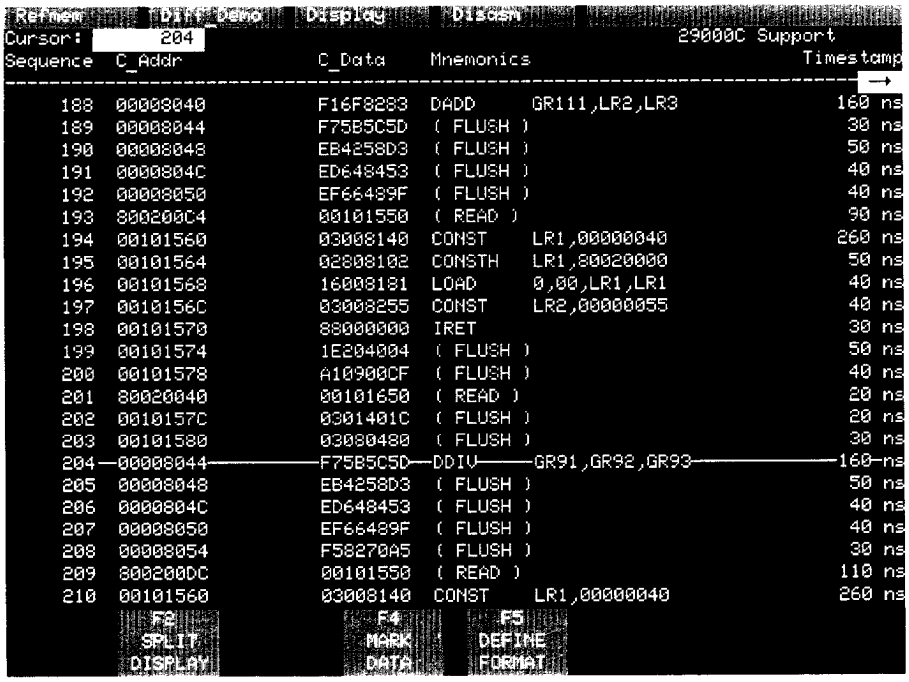


Figure 4-15. Floating point instructions displayed for the Am29000.
This data is not from the 29000_Demo reference memory file.

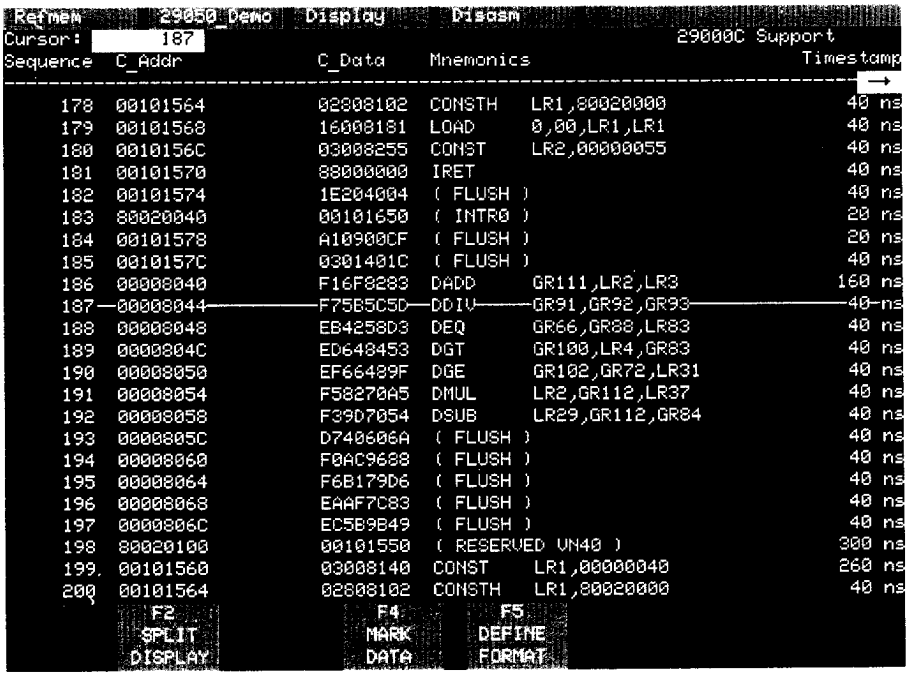


Figure 4-16. Floating point instructions displayed for the Am29050.
This data is from the 29050_Demo reference memory file.

Displaying the C_Addr and D_Addr Groups Symbolically

The C_Addr and D_Addr groups can be displayed as symbol values similar to the way the C_Ctrl, C_Intr, and D_Ctrl groups can be displayed as symbol values. You can use the Symbol Editor menu to create symbol tables to assign symbols to specific addresses or various address ranges; then use the Channel menu to change the default radix of the C_Addr or D_Addr groups to SYM and assign to it the symbol table. All effective addresses are sent to the table before being displayed. Refer to your *DAS 9200 System User's Manual* for a description of how to create symbol tables.

You can also change the radix of the C_Addr or D_Addr group to SYM in the Disassembly Format Definition overlay. Figure 4-17 shows an example of the C_Addr group displayed symbolically. The symbol table file used for the C_Addr group in this figure is the 29000_Demo symbol file. It is only valid for the 29000_Demo reference memory file.

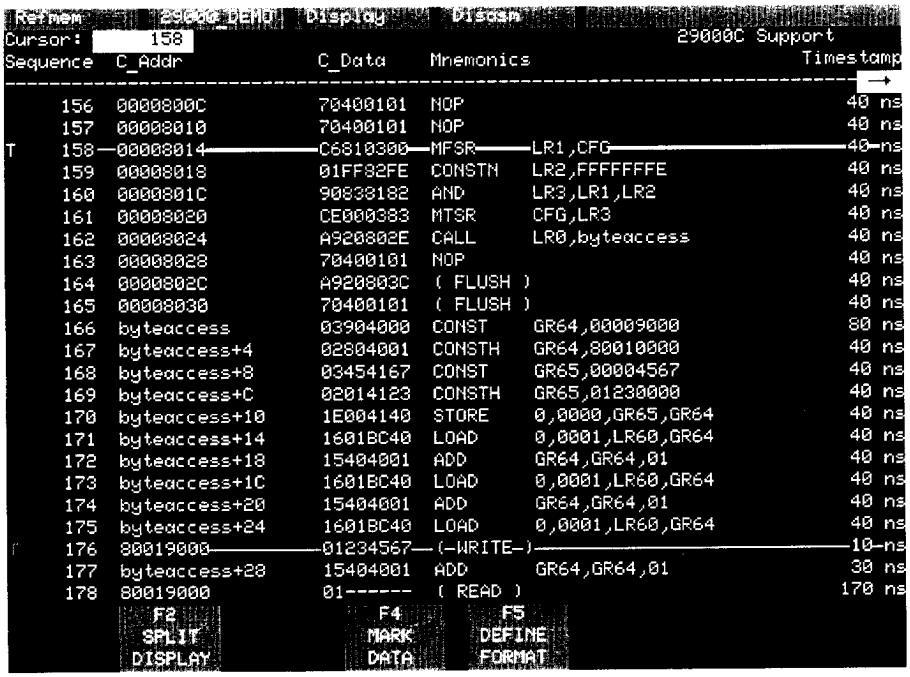


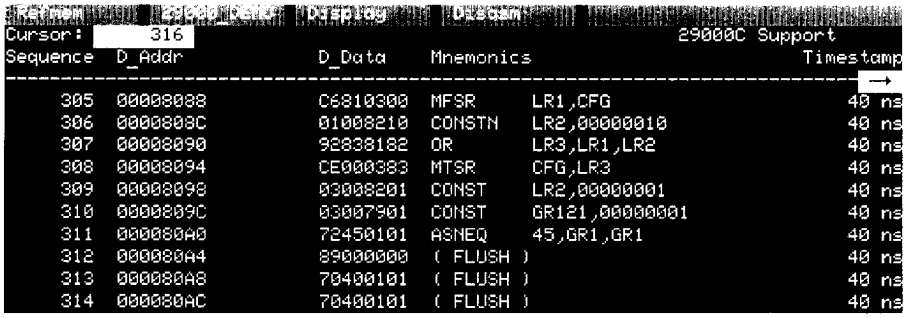
Figure 4-17. C_Addr group displayed symbolically.

Defining and Using the Vector Area

Interrupt and trap processing rely on the existence of a user-managed Vector Area. This area begins at an address specified by the Vector Area Base Address Register. The Vector Area has one of two possible structures: a table of individual vectors or segments of contiguous blocks of instructions.

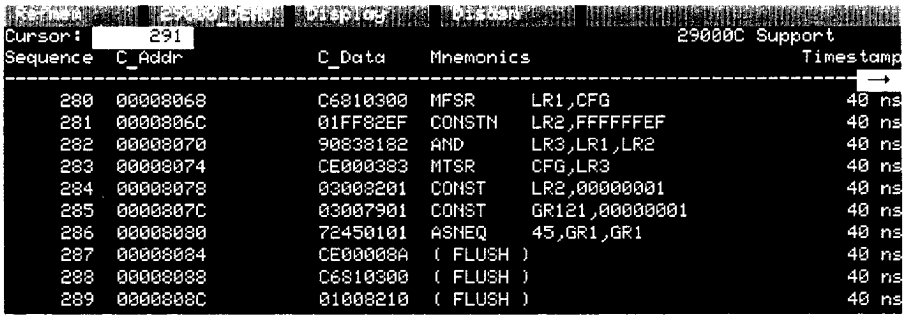
The locations of these tables are defined by the Am29000/050 system software. By setting the vector type and vector base in the disassembler to match that of the Am29000/050 system, disassembly of these vectors will be correct. You can enter the type of vector table, as well as the specific address in which it is located in your Am29000/050 system, through two fields in the Disassembly Format Definition overlay. These fields are the Vector Area Type and Vector Area Base fields. Refer to the description of this overlay for details on using these vector fields.

Figure 4-18 shows how a specific Vector Address is displayed. Figure 4-19 shows how an Instruction Block is displayed.



```
Cursor:    316                                          29000C Support
Sequence  D_Addr          D_Data    Mnemonics                    Timestamp
-------------------------------------------------------------------------→
     305  00008088        C6810300  MFSR     LR1,CFG                  40 ns
     306  0000808C        01008210  CONSTN   LR2,00000010             40 ns
     307  00008090        92838182  OR       LR3,LR1,LR2              40 ns
     308  00008094        CE000383  MTSR     CFG,LR3                  40 ns
     309  00008098        03008201  CONST    LR2,00000001             40 ns
     310  0000809C        03007901  CONST    GR121,00000001           40 ns
     311  000080A0        72450101  ASNEQ    45,GR1,GR1               40 ns
     312  000080A4        89000000  ( FLUSH )                         40 ns
     313  000080A8        70400101  ( FLUSH )                         40 ns
     314  000080AC        70400101  ( FLUSH )                         40 ns
```

Figure 4-18. Vector Address.



```
Cursor:    291                                          29000C Support
Sequence  C_Addr          C_Data    Mnemonics                    Timestamp
-------------------------------------------------------------------------→
     280  00008068        C6810300  MFSR     LR1,CFG                  40 ns
     281  0000806C        01FF82EF  CONSTN   LR2,FFFFFFEF             40 ns
     282  00008070        90838182  AND      LR3,LR1,LR2              40 ns
     283  00008074        CE000383  MTSR     CFG,LR3                  40 ns
     284  00008078        03008201  CONST    LR2,00000001             40 ns
     285  0000807C        03007901  CONST    GR121,00000001           40 ns
     286  00008080        72450101  ASNEQ    45,GR1,GR1               40 ns
     287  00008084        CE00008A  ( FLUSH )                         40 ns
     288  00008088        C6810300  ( FLUSH )                         40 ns
     289  0000808C        01008210  ( FLUSH )                         40 ns
```

Figure 4-19. Instruction Block.

You can re-create these figures on your DAS 9200 using the 29000_Demo reference memory. To re-create Figure 4-18, follow these steps:

1. Enter 316 in the Cursor field.
2. Press the Return key. The cursor will move to sequence 316.
3. Press F5: DEFINE FORMAT.
4. Move the cursor to the Vector Area Base field and enter 80000000. This is the starting address of the vector table in the reference memory file.
5. Move the cursor to the Vector Area Type field and select Vector Addresses.
6. Press the Return key.
7. Press F8: EXIT & SAVE.

To re-create Figure 4-19, follow these steps:

1. Enter 291 in the Cursor field.
2. Press the Return key. The cursor will move to sequence 291.
3. Press F5: DEFINE FORMAT.
4. Move the cursor to the Vector Area Base field and enter 00010000. This is the starting address of the vector table in the reference memory file.
5. Move the cursor to the Vector Area Type field and select Vector Block.
6. Press the Return key.
7. Press F8: EXIT & SAVE.

Moving the Cursor to Suppressed Sequences

When displaying data in Software, Control Flow, or Subroutine formats, some sequence location numbers will be suppressed. You can still enter a specific sequence location number that has been suppressed. The cursor moves to the sequence nearest the suppressed sequence that can be displayed. If there is a large block of suppressed sequences near the desired sequence, there can be a noticeable delay while the system searches for a sequence that can be displayed.

Marking Cycles

You can mark a data sample to easily identify data samples, to move quickly to a data sample, to manually correct a disassembled bus cycle, or to calculate delta timestamp measurements. You can mark a data sample with an A through M, a delta mark (Δ), or the correct bus cycle using the F4: MARK DATA feature of the Disassembly menu. An "m" is placed next to any sample that has had the bus cycle manually changed with an opcode mark.

An Undo Mark selection is also available for opcode marks. You can use both data and opcode marks on a data sample.

You can only change opcodes on data samples from the C_Bus module.

Manually Overriding Disassembled Instructions

Although the disassembler generally disassembles bus cycles correctly, there are situations where disassembled bus cycles are invalid. This is likely to occur at the beginning of an acquisition when the disassembler is not acquiring enough Am29000/050 information to accurately disassemble the bus cycles. After a few samples are acquired, however, enough information is present to enable the disassembler to begin correctly disassembling the bus cycles. Similar situations can also occur after a reset, at the end of an acquisition, when using storage qualification in the Trigger menu, after an instruction that has caused a branch, or when FMACC, DMACC, MTACC, or MFACC exceptions occur and the ACF bits of the FPE register equals 00 or 11.

To manually correct invalid disassembly, you can use the F4: MARK DATA key to change an erroneously disassembled bus cycle. You can mark a program fetch cycle as one of two different opcodes. Table 4-2 shows the opcode selections and their functions when used to correct the invalid disassembly. The disassembler will not let you change non-program fetch cycles such as a read or write.

Table 4-2
Opcode Mark Selections

Opcode Mark	Function
Flush	The cycle is defined as a flushed instruction (unexecuted)
Opcode	The cycle is defined as the start of an instruction
Undo Mark	Removes the opcode mark from the sample on which the cursor is currently positioned

To correct a bus cycle, follow these steps:

1. Place the cursor on the data sample you want to change in the Disassembly menu.
2. Press F4: MARK DATA and select a bus cycle type.

   When you press F4: MARK DATA, a list of selections appears. The list will change from sample to sample to reflect logical opcode or data mark selections for that individual sample. Unlike data marks that can only be used once, opcode marks can be used as often as necessary.

   If the data sample already has an opcode mark on it, then the selection list appears with the cursor on that mark. To remove the opcode mark from the sample on which the cursor is positioned in the Disassembly menu, select Undo Mark.
3. Press the Return key.

The data sample will reflect the corrected bus cycle and other samples may be affected according to the correction. An "m" is placed at the beginning of the data sample that has had the disassembled bus cycle manually changed. Figure 4-20 shows a conditional jump after being corrected using the F4: MARK DATA key.

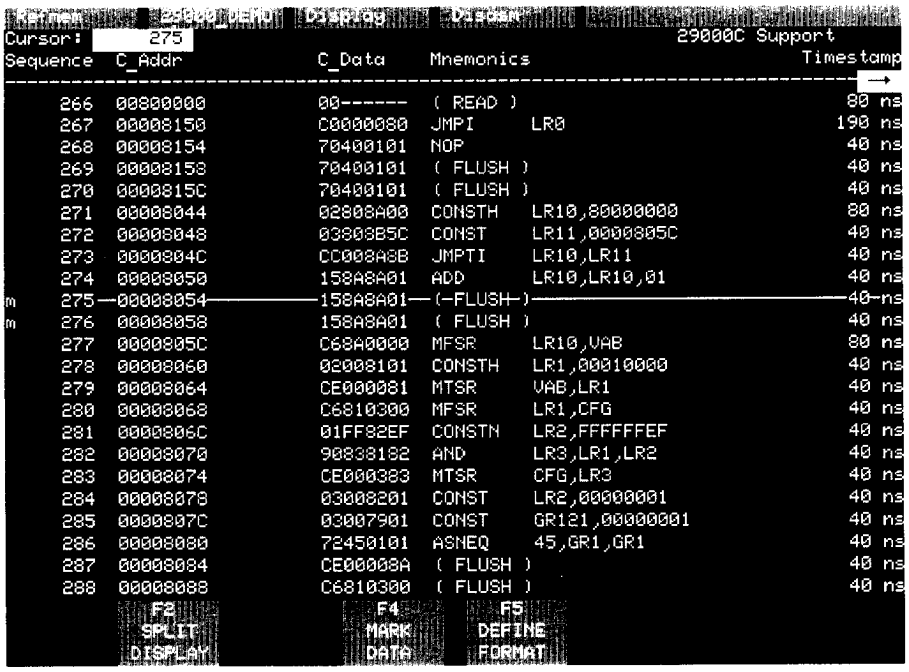


Figure 4-20. A corrected conditional jump after using the F4: MARK DATA key.

Marking a Data Sample

Marks can be used to make data samples easy to identify, and to quickly move the cursor to a marked sample. A special mark, the delta mark (Δ), is also used to calculate delta timestamp values.

The available marks are A through M and Δ. When you mark a data sample, that mark is attached to the acquired data. The mark shows with the data sample in all display menus until you change it. If you are viewing the data in a split-screen display, such as when performing a search, the mark is attached only to the window in which it is placed and will not be carried over to the other window.

A small arrow appears at the beginning of the line of the marked data sample to make the mark more visible. The arrow disappears when both a data mark and an opcode mark are placed on the same sample.

To place a mark on a data sample, follow these steps:

1. Place the cursor on the data sample you want to mark in the Disassembly menu.
2. Press F4: MARK DATA and select a mark.

   When you press F4: MARK DATA, a list of selections appears. The cursor in the selection list will always be on the next unused mark. If you select a mark that has already been used, the previously marked sample will be unmarked and the current sample will be labeled with that mark when you close the selection list. Each mark can only be used on one data sample.
3. Press the Return key.

You can remove all the data marks in the Disassembly menu by using the State menu. To remove all data marks, follow these steps:

1. Press the Select Menu key to return to the Menu Selection overlay.
2. Select the State menu and press the Return key.
3. Press F5: DEFINE FORMAT.
4. Press F2: REMOVE MARKS and press the Return key. All the data marks will disappear.
5. Press the Select Menu key to return to the Menu Selection overlay.

6. Select the Disassembly menu and press the Return key. No data marks appear in the Disassembly menu; they have all been removed.

You can use the Δ mark to make delta timestamp measurements. After placing a Δ mark on a data sample, you can select the Delta selection in the Timestamp field of the Disassembly Format Definition overlay. When you press F8: EXIT & SAVE, the Disassembly menu samples will show the amount of time elapsed between the data sample with the Δ and each previous and subsequent sample.

To quickly move from one data mark to another, enter the mark for the new location in the Cursor field of the Disassembly menu. Enter an ^ in the Cursor field to move the cursor to a Δ mark.

Searching Through Data

The disassembler does not have a Disassembly Search Definition overlay. However, you can effectively search through disassembled data by using the following procedure:

1. Press F2: SPLIT DISPLAY to use the Split-Screen overlay.
2. Select the Disassembly menu for one half of the split-screen display and the State menu for the other half.
3. Press F5: SPLIT HORIZ to split the screen into two horizontal displays.
4. Press F2: LOCK CURSORS. A selection list appears.
5. Select **lock cursors at the same sequence**.
6. Press the Return key.
7. Press F8: EXIT & SAVE to display the menus in a split screen.
8. If the active menu is the Disassembly menu, press F3: SWITCH WINDOW to make the State menu active. The active menu is the one with the yellow cursor and Cursor field.
9. Press F6: DEFINE SEARCH to use the Search function of the State menu to search for the desired sequence.

When searching for data in a clustered module setup in the State menu, the searches are conducted only for the master module. Refer to the description of the State Search Definition overlay in your module user's manual for a description of how to search through state data. Also refer to that manual for a description of how to return to a full screen display.

To abort a search, press the Esc (escape) key.

Figure 4-21 shows the screen split into State and Disassembly windows with the cursors locked on the same bus cycle.

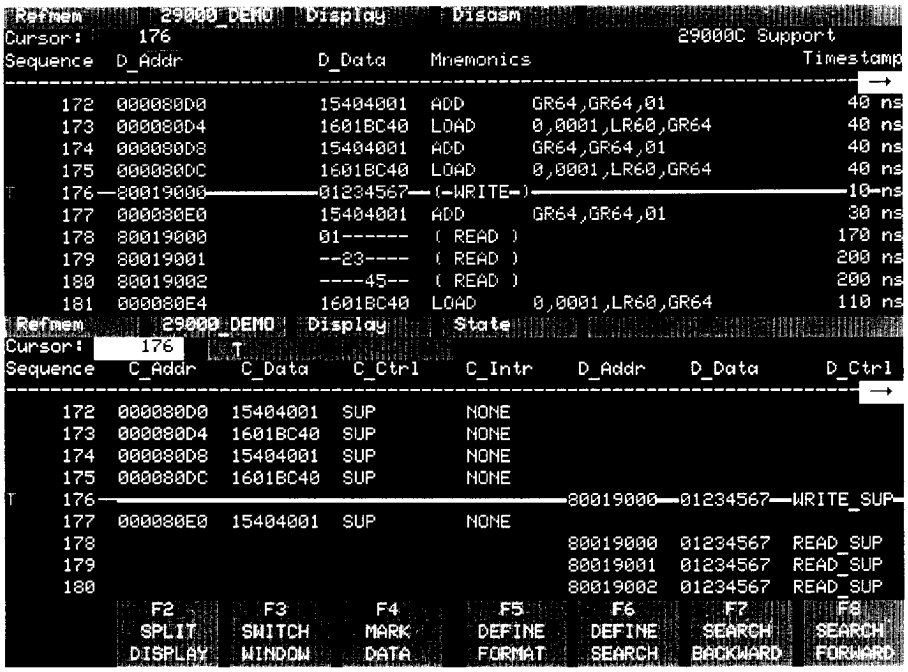


Figure 4-21. State and Disassembly split-screen display used to perform searches.

PRINTING DATA

To print disassembled data, use the Disassembly Print overlay. To access this overlay, press the Shift and Print keys at the same time from the Disassembly menu.

You can choose one of two destinations for the disassembled data: the RS-232 Auxiliary Port, or a file stored on the hard disk. The data is formatted the same in both cases. Appendix C in the *DAS 9200 System User's Manual* contains information on connecting the RS-232 Auxiliary Port to a printer.

If the Send Output To field is set for a file, you need to name the file (the default name is Output). The file is stored in the Print Output directory. This file can be renamed, deleted, copied to a floppy disk, and so on from the Disk Services menu.

If the Send Output To field is set for the RS-232 Auxiliary port, the printer attached to this port receives the data for printing. To set the rate of transmission (baud rate) for the Auxiliary port, select the Communications menu and set the baud rate to match the data rate of your printer.

The parameters you can define in the Disassembly Print overlay are as follows:

- characters per line
- lines per page
- spaces to indent
- new line characters
- new page characters
- comment for page headings
- beginning and ending sequence numbers

If you are using a single module, printed data looks similar to the data displayed on a DAS 9200 terminal screen.

If you are using two or more modules, each sample on the printout has a letter at the beginning of each line (not a data mark). Each letter represents a different module in a cluster. A legend at the top of the printout indicates which module each letter represents.

If the width of the data exceeds the width of the specified line length (maximum 300 characters), greater than symbols (>) are printed to indicate that the data continues past the edge of the page. If you define more characters per line than can fit on a page, the data will either print on the next line or run off the edge of the page, depending on the type of printer being used.

To print the display screen, make the appropriate selections for the Saved Printer Settings (top of the Disassembly Print overlay) and the output specification, and press F5: PRINT. During printing, you can abort the printing sequence at any time by pressing F5: STOP PRINT.

NOTE

The DAS 9200 does not detect printer errors and will not give any error or warning messages if the print sequence cannot be completed.

For information on printer cable connections, refer to Appendix C in your DAS 9200 User's Manual.

Figure 4-22 shows the Disassembly Print overlay.

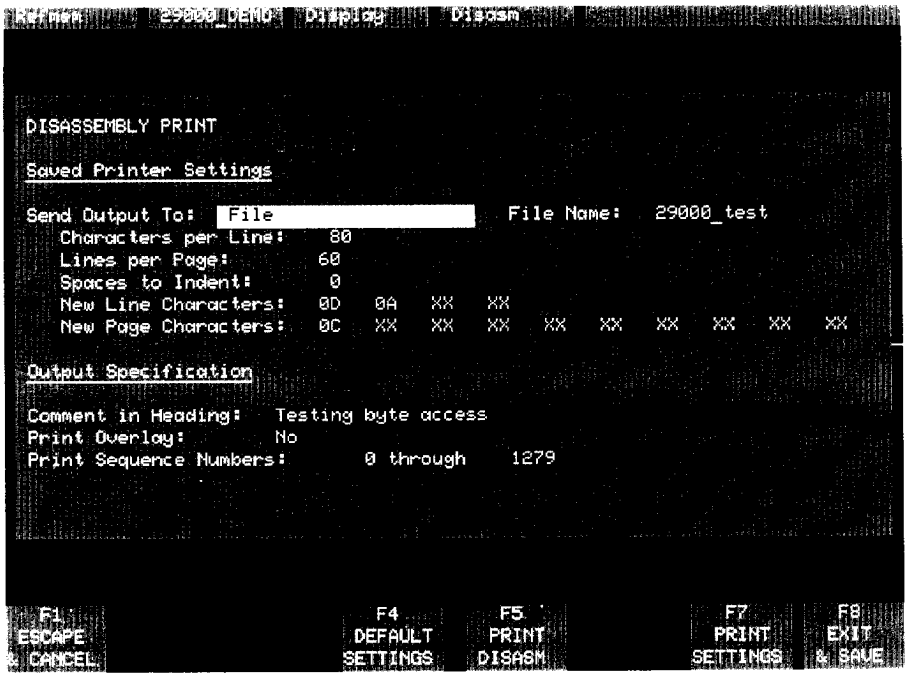


Figure 4-22. Disassembly Print overlay.

Section 5: HARDWARE ANALYSIS

You may need to perform hardware analysis on your Am29000/050 system prior to, during, and after attempting to integrate your software with the Am29000/050 system hardware. When performing hardware analysis, you will want to use the data acquisition module(s) to acquire data with a finer resolution. When more data samples are taken in a given period of time, the resolution in the Timing display increases, and you can see signal activity that would otherwise go undetected.

To acquire and display timing data, you need to select the clocking type, acquire data, and view the data in the Timing menu. Three predefined Timing Format Definition overlay files (with bus forms) called 29000C_96, 29000D_96, and 29000_9696 can be used to view Am29000/050 timing data either on an individual or combined bus basis. A description of these files and how to use them can be found later in this section.

The data acquisition module acquires data from 20 signals that are not necessary for mnemonic disassembly. Some of these signals are meaningful in disassembly and others are only useful for hardware analysis. Appendix B contains a description of these 20 signals and how they can be useful.

If you are not interested in acquiring data from these signals, you can disconnect them from the probe adapter and reconnect the channels (podlets) to other system signals more useful to you. Refer to *Alternate Connections* in Section 3 for information on which channels you can use to make alternate connections between the DAS 9200 and the system under test. Refer to *Disconnecting Clock and 8-Channel Probes* and *Removing and Replacing Podlets* in Appendix C for information on disconnecting probes, and separating the individual podlets from an 8-channel probe.

NOTE

Power down the Am29000/050 system before making alternate connections. Power on the Am29000/050 system after all connections are made. It is not necessary to power down the DAS 9200.

CLOCKING

To change the data sampling rate, use the Clock menu.

When using the 92A96 Module for hardware analysis, you will want to use the Internal or External clocking modes. The Internal clock selection can sample data up to 100 MHz, which has a 10 ns resolution between samples. The External clock selection samples data on every active clock edge on the 92A96 clock inputs up to 100 MHz.

The default Clock menu is shown in Figure 4-2. The default clocking mode is Custom when microprocessor support is used; you will need to change it to either Internal, or External. Your data acquisition module user's manual contains an in-depth description of the Clock menu.

Custom Clocking

Custom clocking only stores one data sample for each bus transaction, which can take one or more clock pulses. This clocking selection is generally unproductive for timing analysis. Refer to Appendix B for a more in-depth description of how Custom clocking acquires data.

Internal Clocking

When you select Internal as the clocking mode, the data acquisition module stores one data sample as often as every 10 ns (100 MHz). Internal clocking sets the 92A96 to sample data based on a clock internal to that module and is commonly called asynchronous.

The disassembly/timing jumper is used in conjunction with clocking selections in the Clock menu. You can view acquired data using Internal clocking (asynchronous) with the jumper in the D position but no data will be seen for the SYSCLK signal. In the D position, the SYSCLK signal, the Am29000/050 system clock signal, can be used as a sampling clock source and is not stored as data.

You can also set the disassembly/timing jumper in the T position. The SYSCLK signal is then acquired as data and can be viewed in the display menus.

Two typical uses of Internal clocking might be to verify that all the Am29000/050 signals are transitioning as expected, or to measure timing relationships between signals.

It is possible to acquire asynchronous data at rates of 200 MHz and 400 MHz. The faster the 92A96 Module acquires data, the fewer channels it can acquire data on. A single 92A96 Module can acquire data on 24 channels at 400 MHz or 2.5 ns resolution. Refer to your *92A96 Module User's Manual* for information on sampling data at speeds faster than 100 MHz.

External Clocking

When you select External as the clocking mode, the data acquisition module acquires and stores data based on the clock channel up to 100 MHz. External clocking sets the 92A96 Module to sample data based on an external clock, in this case, the system clock of the Am29000, and is commonly called synchronous.

The disassembly/timing jumper is used in conjunction with clocking selections in the Clock menu and must be set in the D position when sampling data synchronously with the Am29000/050 system. (Do not use the T position when using External clocking.) You can view acquired data in the Timing menu but no data will be seen for the SYSCLK signal. The SYSCLK signal, the Am29000/050 system clock signal, is not stored as data when using External clocking.

When the disassembly/timing jumper is in the D position, SYSCLK is connected to Clock 1 on the C_Bus module and Clock 0 on the D_Bus module. The data acquisition modules will sample data on every rising edge of SYSCLK when you select the rising edge of Clock 1 on the C_Bus module and the rising edge of Clock 0 on the D_Bus module as the clock channels, and turn off the remaining five clocks. No data is acquired on the falling clock edge unless you select both edges.

You can also use the other three clock channels in each module as clock qualifiers to further modify clocking for your Am29000/050 system.

TRIGGERING

All the Trigger menu selections currently available for that data acquisition module are still valid for hardware analysis. Refer to your module user's manual for a list and description of the selections.

ACQUIRING DATA

You can acquire data as described in the *Acquiring Data* description in Section 4.

DISPLAYING DATA

Hardware analysis requires that you view data in either the State or Timing menus. The following discussion describes these menus.

Timing Menu

In the Timing menu, every channel is shown as an individual waveform, as part of a bus form, or as both.

Three predefined Timing Format Definition overlay files are available for you to use when displaying data in the Timing format. The 29000C_96, 29000D_96, and 29000_9696 files were installed on the DAS 9200 with the disassembler software.

You can use the 29000C_96 timing format file to view data from a single unclustered C_Bus module, the 29000D_96 file to view data from a single unclustered D_Bus module, and the 29000_9696 file to view data from two clustered modules.

Each timing format places the system clock as the first displayed channel followed by other important control signals. Address and data group signals are shown as bus forms containing bus values instead of as individual timing waveforms. Figure 5-1 shows data displayed using the 29000_9696 Timing Format file. This data is not from the 29000_Demo or 29050_Demo reference memory files.

To select a timing format file, follow these steps:

1. Press the Select Menu key to return to the Menu Selection overlay.
2. Select the Timing menu in the Display column.
3. Press the Return key.
4. Press F5: DEFINE FORMAT.
5. Press F5: RESTORE FORMAT.
6. Select 29000C_96, 29000D_96, or 29000_9696, and press the Return key. A message tells you the format file is selected.
7. Press F8: EXIT & SAVE to return to the Timing menu.

Timing data will display in the format described above.

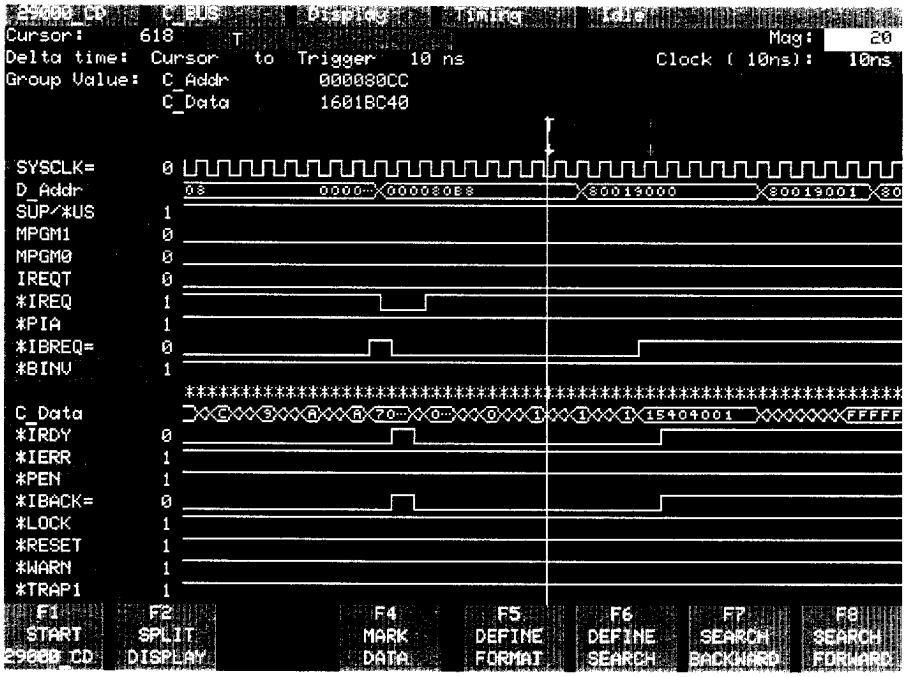


Figure 5-1. Timing data displayed using the 29000_9696 Timing Format. The clocking selection is Internal.

State Menu

In the State menu, all channel group values are shown based on the selected radix in the Channel menu or the State Definition Format overlay. No instruction mnemonics are displayed. Figure 5-2 shows data sampled with External clocking in the State menu. This data is not from the 29000_Demo or 29050_Demo reference memory files.

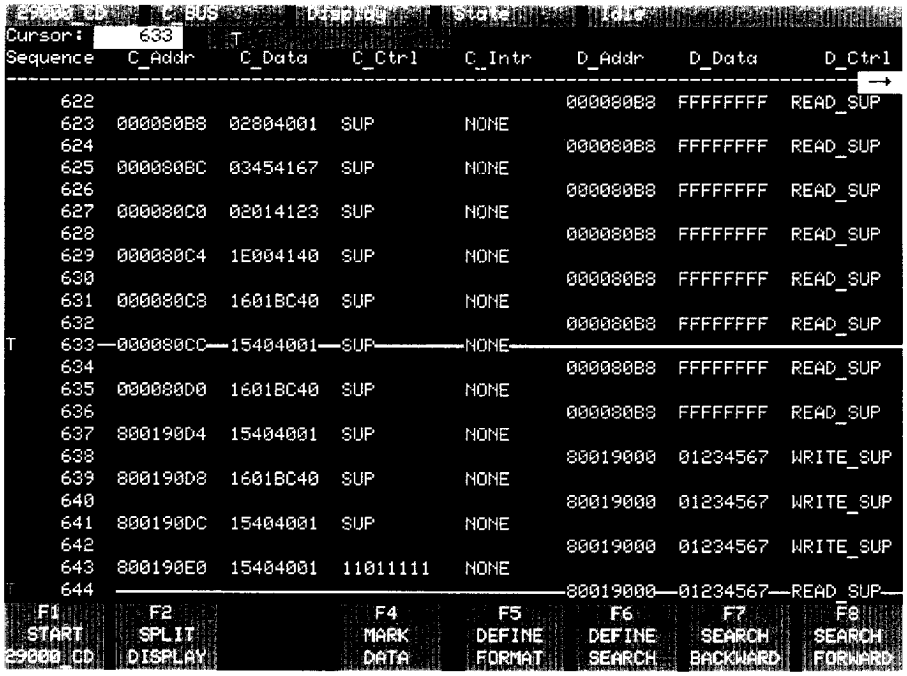


Figure 5-2. State data. The clocking selection is External.

VIEWING AND SEARCHING THROUGH DATA

You can view and search through State and Timing data as described in your module user's manual.

PRINTING DATA

To print state data, you can use the State Print overlay. To print timing data, you can use the Timing Print overlay. To access either print overlay, press the Shift and Print keys at the same time from the State or Timing menu. Refer to your module user's manual for a complete description of these overlays.

Appendix A: ERROR MESSAGES AND DISASSEMBLY PROBLEMS

This section describes error messages and disassembly problems you might encounter while acquiring data.

MODULE ERROR MESSAGES

These error messages will appear in the Module Monitor menu when there are problems with acquiring data or satisfying the trigger program. The error messages are listed in alphabetical order.

Slow Clock

This message appears when the active clock channel (or channels) is not changing or is typically changing at 1 ms or slower intervals, or one of the Am29000/050 clock qualifiers is in the wrong state. Check for the following:

1. The Am29000/050 system is powered on and running. Be sure the system is not halted.
2. A cluster setup is restored in the Save/Restore menu, or that 29000C or 29000D Support is selected in the respective Configuration menu for the C_Bus and D_Bus module.
3. Custom is selected in the Clock menu(s).
4. The connections between the C_Bus (lower-numbered slot) and D_Bus modules and probe adapter are correct.

   The clock and 8-channel probe connections between the interface housings and probe adapter are correct (clock, section names, and channel numbers match), are properly oriented (GND connects to ground), and are fully engaged.
5. The connections between the interface housings and 92A96 probe cables have matched color labels, matched slot numbers, and are properly keyed.
6. The connections between the 92A96 probe cables and probe connectors have matched color labels, matched slot numbers, and are properly keyed.
7. The orientation of pin A-1 on the Am29000/050 in the probe adapter is correct.
8. The lever on the ZIF socket is locked.

9. The disassembly/timing jumper setting on the probe adapter is correct. Set the jumper to D to acquire disassembled data or to T to acquire timing data.
10. The orientation of pin A-1 on the probe adapter in the Am29000/050 system is correct.
11. No bent or missing pins on the Am29000/050 microprocessor or on either of the probe adapter sockets.

Waiting for Stop

This message appears when the trigger condition is satisfied and memory is full but the Manual Stop mode is selected in the Cluster Setup menu. The solution is to manually stop the DAS 9200 by pressing F1: STOP.

This message can also appear when other modules in the cluster have not filled their memories. The solution in this case is to wait for the other modules to fill their memory. If the message does not disappear in a short time, press F1: STOP.

Waiting for Stop-Store

This message appears when the trigger condition is satisfied but the amount of post-fill memory specified in the trigger position field is not yet filled. Press F1: STOP to view the acquired data, then check for the following:

1. The trigger program in the Trigger menu is correct.
2. The storage qualification in the Trigger menu is correct.
3. The system or the module does not have an exception or fault. The Am29000/050 system or data acquisition module might have experienced a hardware or software exception or fault after the trigger condition was satisfied.

Waiting for Trigger

This message appears when the trigger condition doesn't occur. Check for the following:

1. The Am29000/050 system is powered on and running. Be sure the system is not halted.
2. The trigger conditions are being satisfied. The Module Monitor menu shows which state events are not occurring. Press F1: STOP, access the Trigger menu, and redefine the conditions for that state. Also refer to the description on *Triggering* in Section 4.

OTHER DISASSEMBLY PROBLEMS

There may be problems with disassembly for which no error messages are displayed. Some of these problems and their suggested solutions follow:

Incorrect Data

If the data acquired is obviously incorrect, check the following:

1. The orientation of pin A-1 on the Am29000/050 in the probe adapter is correct.
2. The lever on the ZIF socket is locked.
3. The disassembly/timing jumper setting on the probe adapter is correct. Set the jumper to D to acquire disassembled data or to T to acquire timing data.
4. The orientation of pin A-1 on the probe adapter in the Am29000/050 system is correct.
5. No bent or missing pins on the Am29000/050 microprocessor or on either of the probe adapter sockets.

No Data

If no data is displayed after satisfying the trigger program and filling post-fill memory, check the following:

1. The Am29000/050 system is powered on and running. Be sure the system is not halted.
2. Incorrect data qualification is used in the Trigger menu.
3. The trigger program in the Trigger menu is correct.

Other Suggestions

If the previous suggestions don't fix the problem with acquiring disassembled bus cycles or instruction mnemonics, try the following:

1. Restore the cluster setup file from the Save/Restore menu to restore the DAS 9200 to a known state.

   Or, reload the module setup by selecting the 29000C or 29000D Support in the 92A96 Configuration menu for the C_Bus or D_Bus module to restore the DAS 9200 to a known state.

2. Possible ac and dc loading problems may be remedied by removing the ZIF socket from the probe adapter. If this doesn't ease the loading problem sufficiently, you should remove one or both of the protective sockets from the probe adapter. These sockets may add enough additional inductance to your Am29000/050 system to affect it. Refer to Appendix B for a description of the proper way to remove sockets from the probe adapter.

If the DAS 9200 still is not acquiring data after trying these suggestions, there may be a problem with the Am29000/050 system. Try performing hardware analysis with your DAS 9200 system to ensure that the Am29000/050 signals are valid at the time the probe adapter samples them.

Refer to *Section 5: Hardware Analysis* for information on data sampling rates using either the Internal or External clocking selections in the Clock menu. Also refer to *Appendix B: How Data is Acquired* to see when the disassembler samples the various Am29000/050 system signals.

Appendix B:
HOW DATA IS ACQUIRED

This appendix tells how the 92A96 Module acquires Am29000/050 signals. Each 92A96 Module logs in signals from one group of channels at one time, and from another group of channels at a later time. The module then sends all of the logged-in signals to the trigger machine and to acquisition memory for storage.

C_BUS MODULE CUSTOM CLOCKING

The C_Bus module Custom clocking for the Am29000/050 uses three sample points. The first sample point is at the beginning of a bus cycle where the high-order bits of the Address bus (A31–A12) and various control signals are logged in. The second sample point occurs at the end of a bus cycle where the Instruction bus and the remaining control signals are logged in. The third sample point also occurs at the end of a bus cycle where the low-order bits of the Address bus (synthesized address signals A11–A0) are logged in. The third and last sample point in each bus cycle also generates the master clock which sends all logged data to the trigger machine and acquisition memory. Figure B-1 shows these three sample points and the master clock. View A shows the sample points with one wait state; view B shows the sample points with no wait states.

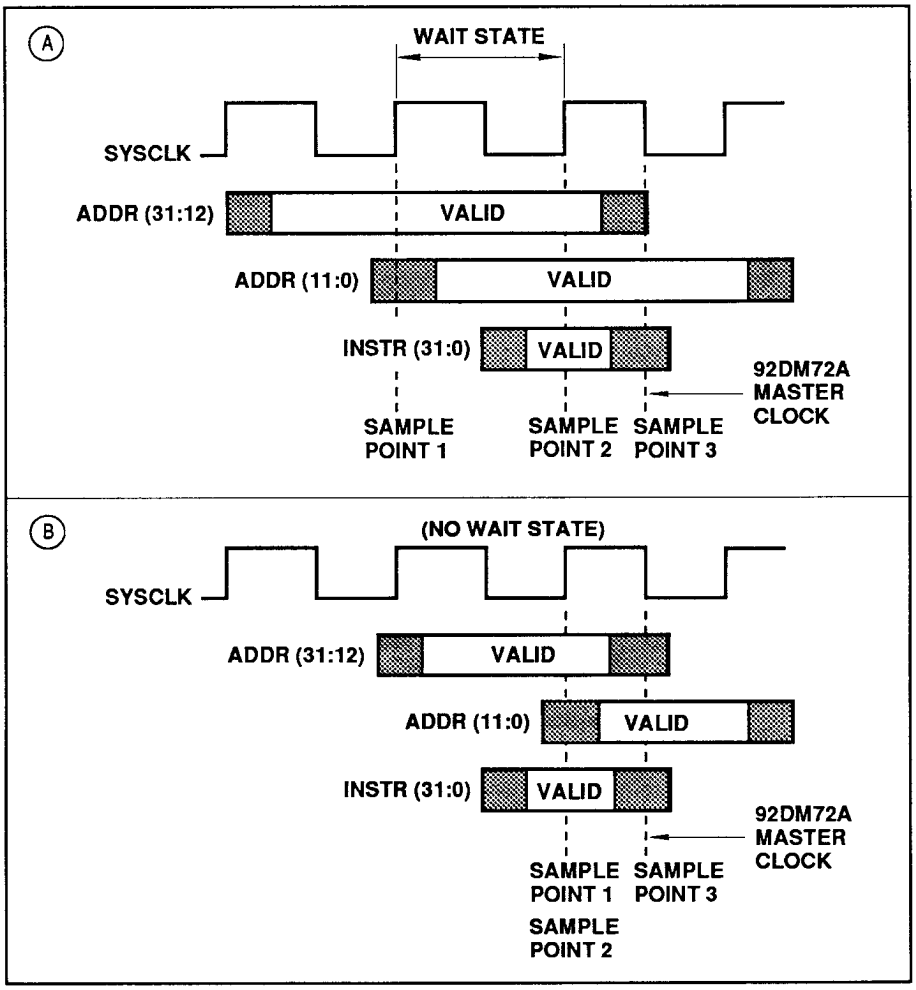


Figure B-1. C_Bus module bus timing. The 92DM72A samples code bus signals at the points shown above. When the 92A96 master clock occurs, the sampled signals are combined to form one complete data acquisition record.

Table B-1 shows what signals are acquired at each sample point shown in Figure B-1.

Table B-1
C_Bus Sample Points

Sample Point	Signals Acquired
1	A31–12, *BINV, *INTR0, *INTR3,*IREQ, IREQT, *LOCK, MPGM0, MPGM1, *PEN. *PIA, *RESET ,SUP/*US, *TEST, *TRAP1
2	C_DATA, CNTL0, CNTL1, *IBACK, *IBREQ, *IERR, *IRDY, *INTR1, *INTR2, MSERR, STAT0, STAT1, STAT2, *TRAP0, *WARN
3	A11–0

When the microprocessor is fetches an instruction for every clock cycle with no wait states, the first two sample points occur at the same time. When wait states occur, the first two sample points are separated in time. The Custom clocking algorithm takes care of wait states by not logging in any data during them.

After the acquisition is complete, the disassembler reads the acquisition memory. Since each memory location contains data for a complete bus cycle, the disassembler is able to deduct the kind of bus activity that took place. For example, if an opcode fetch occurred, the disassembler converts the 92A96 data bus into the opcode the data bus represents.

D_BUS MODULE CUSTOM CLOCKING

The D_Bus module Custom clocking for the Am29000/050 uses two sample points. The first sample point is at the beginning of the cycle where the entire Address bus (A31–A0) and various control signals are logged in. The second sample point occurs at the end of a bus cycle where the Data bus and the remaining control signals are logged in. The second and last sample point in each bus cycle also generates the master clock, which sends all logged data to the trigger machine and acquisition memory.

Figure B-2 shows these two sample points and the master clock. View A shows the sample points with one wait state; view B shows the sample points with no wait states.

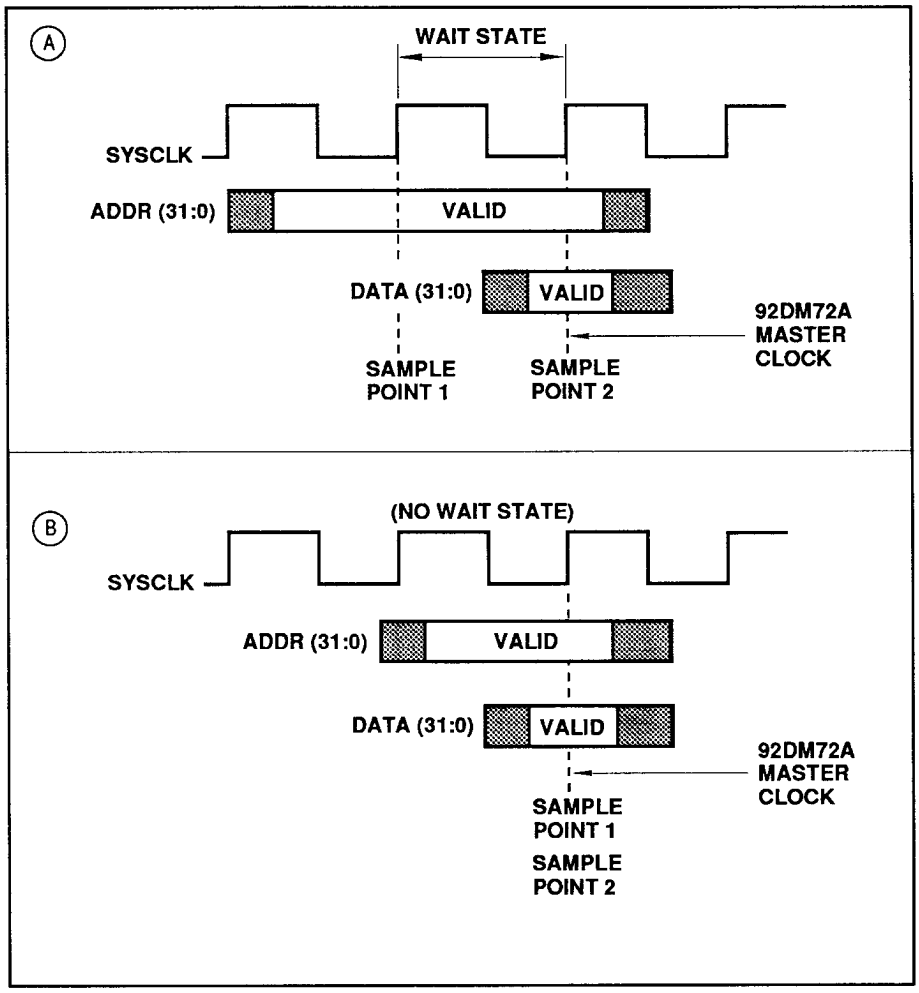


Figure B-2. D_Bus module bus timing. The 92DM72A samples data bus signals at the points shown above. When the 92A96 master clock occurs, the sampled signals are combined to form one complete data acquisition record.

Table B-2 shows what signals are acquired at each sample point shown in Figure B-2.

Table B-2
D_Bus Sample Points

Sample Point	Signals Acquired
1	B/*L, B_DREQ, *BGRT, *BINV, *BREQ, D_ADDR, *DREQ, DREQT0, DREQT1, *LOCK, OPT0, OPT1, OPT2, *RESET, R/*W, SUP/*US
2	*CDA, *DBACK, *DBREQ, D_DATA, *DERR, *DRDY, *PDA

Handling of wait states and operation of the disassembler are the same as described for the C_Bus module.

CUSTOM CLOCKING

The Custom clocking algorithm has two variations: DMA cycles included or DMA cycles excluded.

DMA Cycles Excluded

Whenever the D_Bus module is about to log in the first sample of a bus cycle and detects that the Am29000/050 has asserted the *BGRT and *BINV signals, no data is logged in. No bus cycles will be acquired until the Am29000/050 deasserts *BGRT.

DMA Cycles Included

Whenever the D_Bus module is about to log in the first sample of a bus cycle and detects that the Am29000/050 has asserted the *BGRT and *BINV signals, a BUS_GRANT cycle is logged in. All bus cycles are acquired, including those driven by an alternate device which has been granted the bus. The D_Bus module can only sample data at the Am29000/050 pins. To properly log in bus activity driven by alternate bus devices, any buffers between the Am29000/050 and the alternate bus driver must be enabled and pointed towards the Am29000/050. Possible Am29000/050 hardware and clocking interactions are as follows:

- If the alternate device drives the same control lines as the Am29000/050 and the Am29000/050 sees these signals, alternate device bus activity is logged in just like normal bus cycles except that *BGRT will be asserted.
- If none of the control lines are driven or if the Am29000/050 cannot see them, the D_Bus module will still log in a BUS_GRANT cycle when *BGRT if first asserted. However, the actual DMA cycles cannot be acquired.
- If some of the Am29000/050 control signals are visible, the D_Bus module logs in what it determines is valid from the visible control signals.

SIGNALS

The Am29000/050 probe adapter connects to Am29000/050 signals and enables the 92A96 Modules to acquire them. The disassembler software uses the signal information to disassemble the program executing on your Am29000/050 system. The probe adapter must synthesize 14 signals in order to acquire valid data. Not all acquired Am29000/050 signals are needed by the disassembler software for disassembly.

Synthesized Signals

The probe adapter synthesizes 14 signals; Table B-3 describes them. Refer to the previous discussions on *Custom Clocking* and the probe adapter description in Appendix C for a description of how these signals are used.

Table B-3
Synthesized Signals

Signal	Description
C_Bus Module	
Addr_11D, Addr_10D	Latched during early part of the bus cycle. Held during burst access.
Addr_9D– Addr_2D	Latched during early part of the bus cycle. Count during burst access.
Addr_1D, Addr_0D	Grounded on the probe adapter.
D_Bus Module	
B-DREQ	This signal is high when both *DREQ and DREQT1 are low. Used to block acquisition of coprocessor bus transactions.
B/*L	Connected to Vcc (+15 V) when the byte order jumper is in the B position; connected to GND (ground) when the byte order jumper is in the L position.

Signals Not Used for Disassembly

The *Am29000 32-Bit Streamlined Instruction Processor User's Manual* (Advanced Micro Devices, 1988), the *Am29050 Streamlined Instruction Microprocessor Advance Information Manual* (1990), and the *Am29050 Microprocessor User's Manual* (1991) describe the acquired Am29000/050 signals. Some of these signals are not used for disassembly, but may be useful for viewing in the State menu or when performing hardware analysis. Table B-4 shows these signals and their uses.

Table B-4
Signals Not Used for Disassembly

Signal	Use
C_Bus Module	
MPGM1, MPGM0, *IBACK=	Useful for State display and hardware analysis. Default setting is Off in the State menu.
*PIA, *IBREQ=, *PEN, *TEST, STAT2, STAT1, STAT0, CNTL1, CNTL0, MSERR	Useful in hardware analysis. May not be logged in at the correct time when Custom Clocking is used. Default setting is Off in the State menu.
D_Bus Module	
*DREQ, *DRDY=, *DBACK=, *BREQ	Useful for the State display and hardware analysis. Default setting is Off in the State menu.
*PDA, *DBREQ=, *CDA	Useful in hardware analysis. May not be logged in at the correct time when Custom Clocking is used. Default setting is Off in the State menu.
*WARN, *TRAP1, *TRAP0, *INTR3, *INTR2, *INTR1, *INTR0	Useful for State and Disassembly display. Default setting is Off in the State menu.

Refer to *Section 5: Hardware Analysis* for a description of Internal and External clocking choices. Refer also to *Alternate Connections* in Section 3 to learn how to use these channels to make connections to other more useful signals in your Am29000/050 system.

Warning

The following servicing instructions are for use only by qualified personnel. To avoid personnel injury, do not perform any servicing other than that contained in the operating instructions unless you are qualified to do so. Refer to General Safety Summary and Service Safety Summary prior to performing any service.

Appendix C:
SERVICE INFORMATION

This appendix contains the following information:

- safety summary
- brief description of the 92DM72A probe adapter and how it works
- care and maintenance
- specification tables
- channel assignment tables
- minimum clearances for the probe adapter with all seven clock probes and twenty-three 8-channel probes connected
- removing clock and 8-channel probes from the probe adapter
- removing and replacing individual podlets
- removing and replacing sockets
- replaceable electrical parts list
- circuit board component location diagrams
- schematics
- replaceable mechanical parts list
- exploded mechanical diagram

SERVICING SAFETY INFORMATION

The following service safety information is for service technicians. Follow these safety precautions, andthe general precautions outlined in your DAS 9200 acquisition module user's manual while installing or servicing this product.

Do Not Service Alone. Do not perform internal service or adjustment on this product unless another person is present and able to give first aid and resuscitation.

Use Care When Servicing With Power On. To avoid personal injury from dangerous voltages, remove jewelry such as rings, watches, and other metallic objects before servicing. Do not touch the product's exposed connections and components while power is on.

PROBE ADAPTER DESCRIPTION

The probe adapter is a non-intrusive piece of hardware that allows the DAS 9200 to acquire data from an Am29000/050 microprocessor system in its own operating environment with little effect, if any, on that system. The probe adapter adds minimum loading to the Am29000/050 system, and does not intercept, modify, and send signals back to the system. The probe adapter consists of a circuit board with a ZIF socket for the Am29000/050 microprocessor and a small amount of active circuitry.

If you are using only one module, it is called the C_Bus module when it is being used to acquire data from the instruction bus. It is called the D_Bus module when it is being used to acquire data from the data bus. When acquiring data from only the C_Bus module, the probe adapter connects to three clock and twelve 8-channel probes. When acquiring data from only the D_Bus module, the probe adapter connects to four clock and eleven 8-channel probes.

If your are using two modules, the module in the lower-numbered slot acquires data from the instruction bus and is called the C_Bus module. The other module acquires data from the data bus and is called the D_Bus module. The probe adapter connects to seven clock and twenty-three 8-channel probes.

Most signals from the Am29000/050 system flow from the probe adapter directly to square pins connected to the 92A96 clock and 8-channel probes. The signals then go across the 92A96 probe cables to the 92A96 Data Acquisition Module.

Some circuitry is used to synthesize an address for the code module to use during burst mode accesses. This circuitry includes an 8-bit counter that increments the address during a burst of instruction fetches. Address lines A11 through A0 connect to this circuit and synthesize the address that lets the C_Bus module acquire and trigger on all instruction fetch addresses, even though the microprocessor only provides a starting address for each burst of instruction fetches. The D_Bus module connects directly to the address bus on the Am29000/050.

The probe adapter does not acquire bus transactions between the Am29000 microprocessor and the Am29027 coprocessor. The *DREQ signal is combined with DREQT1 to generate B-DREQ. The data module then uses this signal as a clock qualifier to block acquisition of coprocessor bus transactions.

All circuitry on the probe adapter is powered from the SUT.

The probe adapter accommodates the Advance Micro Devices Am29000/050 microprocessor in a 169-pin PGA package. The probe adapter replaces the microprocessor in the SUT and the microprocessor is then placed back in the ZIF socket on the top of the probe adapter.

The probe adapter contains two jumpers, the byte order jumper and the acquisition clock jumper. The byte order jumper determines how the disassembler software organizes memory, either as Big- or Little-Endian byte order.

The acquisition mode jumper can be set in either the D position for acquiring disassembly mnemonics or in the T position to acquire timing data. In the D position, the SYSCLK signal connects to one acquisition clock probe on each module. In this mode, the SYSCLK signal is used only to clock data and is not acquired as data. In the T position, the SYSCLK signal connects to a data probe on each module. In this mode, the module clocks internally and SYSCLK can be acquired and stored as data.

The *WARN and *RESET signals are acquired by the modules and sent to pins on the probe adapter for you to use with other prototype debugging tools. Signals INCLK, PWRCLK, and PIN169 are not acquired but are also sent to pins to make them accessible.

CARE AND MAINTENANCE

The probe adapter does not require scheduled or periodic maintenance. To maintain good electrical contact, keep the probe adapter free of dirt, dust and contaminants. Also, ensure that any electrically conductive contaminants are removed.

Dirt and dust can usually be removed with a soft brush. For more extensive cleaning, use only a damp cloth. Abrasive cleaners and organic solvents should never be used.

CAUTION

The semiconductor devices contained on the probe adapter are susceptible to static-discharge damage. To prevent damage, service the probe adapter only in a static-free environment.

Always wear a grounding wrist strap, or similar device, while servicing the instrument.

Discharge stored static electricity from the probe adapter by touching any of the ground pins (row of square pins closest to the edge of the probe adapter circuit board).

CAUTION

Exercise care when soldering on a multilayer circuit board. Excessive heat can damage the through-hole plating or lift a run or pad and damage the board beyond repair. Do not apply heat for longer than three seconds. Do not apply heat consecutively to adjacent leads. Allow a moment for the board to cool between each operation.

If you must replace an electrical component on a circuit board, exercise extreme caution while desoldering or soldering the new component. Use a pencil-type soldering iron of less than 18 watts and an approved desoldering tool. Ensure that the replacement is an equivalent part by comparing the description as listed in the replaceable parts list.

SPECIFICATIONS

These specifications are for a 92DM72A Probe Adapter connected to two 92A96 Data Acquisition Modules and the SUT. Tables C-1 and C-2 show the electrical and physical specifications for the 92DM72A microprocessor support package and its associated options. Table C-3 shows the environmental specifications.

Table C-1
Electrical Specifications

Characteristics	Requirements	
SUT DC Power Requirement		
Voltage	+5 V ± 0.5 V	
Current	<250 mA max	
SUT Clock		
Clock Rate	33 MHz max.	
Clock Pulse Width†		
Low Time	5 ns min.	
High Time	5 ns min.	
Minimum Setup Time‡		
*IREQ, *IRDY	7 ns	
*PIA, *DREQ, DREQT1	13 ns	
*BINV, #IERR, *DERR, *DBACK	6.5 ns	
All other signals	5 ns§	
Minimum Hold Time‡		
All:2	1 ns	
All other signals	0 ns	
Maximum SUT Signal Loading	AC Load	DC Load
Address Bus		
A31:A12	<30 pF	50 kΩ
A11:2	<30 pF	100 kΩ & 1 74FXX load
A1:0	<25 pF	100 kΩ
Data Bus		
D31:0	<20 pF	100 kΩ
Instruction Bus		
I31:0	<20 pF	100 kΩ
Control		
SYSCLK	<45 pF	50 kΩ & 2 74FXX loads

(Cont.)

Table C-1 (Cont.)
Electrical Specifications

Characteristics	Requirements	
Control (Cont.)	AC Load	DC Load
MPGM1:0, IREQT, STAT2:0, MSERR, *IERR, *CDA, *TRAP1:0, *INTR3:0, *PEN, CNTL1:0,*TEST, OPT2:0, *PDA, DREQT0, R/*W, *DERR, *BREQ, *CDA, *WARN	<25 pF	100 kΩ
SUP/*US, *LOCK, *IBREQ, *BINV, *IBACK, *DBREQ, *DBACK, *BGRT, *DRDY, *RESET	<30 pF	50 kΩ
*PIA, *IRDY, *DREQ, DREQT1	<30 pF	100 kΩ & 1 74FXX load
*IREQ	<30 pF	100 kΩ & 2 74FXX loads
INCLK, PWRCLK, PIN169	<15 pF	

†In order to meet setup and hold requirements as shown in this table, the clock pulse widths will need to be substantially larger than the minimum value shown here.

‡ Setup and hold times are with respect to the rising edge of SYSCLK.

§ Possible timing violations when probing a 33 MHz Am29000/050.

Table C-2
Physical Specifications

Characteristics	Requirements
Overall Cable Length From the DAS 9200 to the tips of the 8-channel probes including the interface housing	5 ft. 10.5 in ≈179 cm
Weight	5.0 oz (≈141 gm)

Table C-3
Environmental Specifications

Characteristic	Description
Temperature	
Max. Operating	+50° C (+122° F)
Min. Operating	+0° C (+32° F)
Non-Operating	-62° C to +85° C (-78° F to +185° F)
Humidity	0–95% relative humidity (non-condensing)
Altitude	
Operating	15,000 ft. (4.5 km) maximum
Non-Operating	50,000 ft. (15 km) maximum
Electrostatic Immunity	The probe adapter is static-sensitive

Table C-4 shows the 92A96 section and channel assignments, their grouping and radix for the disassembler, the voltage threshold, polarity, and microprocessor signal and pin connections for the C_Bus module.

Table C-4
92DM72A Channel Assignments (C_Bus Module)

92DM72A Group (Radix)	Group Bit Pos	92A96 Section: Channel	Voltage Threshold, Polarity	Am29000/050 Signal Name	169-Pin PGA
C_Addr (Hex)	31	A3: 7	TTL, +	A31	D-15
	30	A3: 6	TTL, +	A30	B-17
	29	A3: 5	TTL, +	A29	C-17
	28	A3: 4	TTL, +	A28	D-16
	27	A3: 3	TTL, +	A27	E-16
	26	A3: 2	TTL, +	A26	D-17
	25	A3: 1	TTL, +	A25	F-15
	24	A3: 0	TTL, +	A24	F-16
	23	A2: 7	TTL, +	A23	E-17
	22	A2: 6	TTL, +	A22	G-15
	21	A2: 5	TTL, +	A21	F-17
	20	A2: 4	TTL, +	A20	G-16
	19	A2: 3	TTL, +	A19	G-17
	18	A2: 2	TTL, +	A18	H-16
	17	A2: 1	TTL, +	A17	H-17
	16	A2: 0	TTL, +	A16	J-16
	15	A1: 7	TTL, +	A15	J-15
	14	A1: 6	TTL, +	A14	J-17
	13	A1: 5	TTL, +	A13	K-17
	12	A1: 4	TTL, +	A12	K-16
	11	A1: 3	TTL, +	A11†	L-17
	10	A1: 2	TTL, +	A10†	L-16
	9	A1: 1	TTL, +	A9†	P-17
	8	A1: 0	TTL, +	A8†	P-16
	7	A0: 7	TTL, +	A7†	R-17
	6	A0: 6	TTL, +	A6†	R-16
	5	A0: 5	TTL, +	A5†	P-15
	4	A0: 4	TTL, +	A4†	T-17

(Cont.)

Table C-4 (Cont.)
92DM72A Channel Assignments (C_Bus Module)

92DM72A Group (Radix)	Group Bit Pos	92A96 Section: Channel	Voltage Threshold, Polarity	Am29000/050 Signal Name	169-Pin PGA
C_Addr (Cont.)	3	A0: 3	TTL, +	A3†	T-16
	2	A0: 2	TTL, +	A2†	R-15
	1	A0: 1	TTL, +	A1†	M-17
	0	A0: 0	TTL, +	A0†	M-16
C_Data (Hex)	31	D3: 7	TTL, +	I31	N-1
	30	D3: 6	TTL, +	I30	M-2
	29	D3: 5	TTL, +	I29	M-1
	28	D3: 4	TTL, +	I28	L-2
	27	D3: 3	TTL, +	I27	L-1
	26	D3: 2	TTL, +	I26	K-1
	25	D3: 1	TTL, +	I25	K-2
	24	D3: 0	TTL, +	I24	J-2
	23	D2: 7	TTL, +	I23	J-1
	22	D2: 6	TTL, +	I22	H-2
	21	D2: 5	TTL, +	I21	H-3
	20	D2: 4	TTL, +	I20	H-1
	19	D2: 3	TTL, +	I19	G-1
	18	D2 2	TTL, +	I18	G-2
	17	D2: 1	TTL, +	I17	G-3
	16	D2: 0	TTL, +	I16	F-1
	15	D1: 7	TTL, +	I15	F-2
	14	D1: 6	TTL, +	I14	F-3
	13	D1: 5	TTL, +	I13	E-1
	12	D1: 4	TTL, +	I12	E-2
	11	D1: 3	TTL, +	I11	D-1
	10	D1: 2	TTL, +	I10	D-2
	9	D1: 1	TTL, +	I9	C-1
	8	D1: 0	TTL, +	I8	C-2
	7	D0: 7	TTL, +	I7	D-3
	6	D0: 6	TTL, +	I6	B-1
	5	D0: 5	TTL, +	I5	B-2
	4	D0: 4	TTL, +	I4	C-3
	3	D0: 3	TTL, +	I3	B-3
	2	D0: 2	TTL, +	I2	C-4
	1	D0: 1	TTL, +	I1	A-2
	0	D0: 0	TTL, +	I0	A-3
C_Ctrl (Sym)	7	C2: 3	TTL, +	*IREQ	U-9
	6	C2: 1	TTL, +	*IRDY	T-4
	5	C3: 3	TTL, +	IREQT	U-15
	4	C3: 2	TTL, +	SUP/*US	T-14
	3	C2: 7	TTL, +	*LOCK	T-11
	2	C0: 4	TTL, +	*RESET	R-1
	1	C2: 0	TTL, +	*IERR	U-3
	0	C2: 2	TTL, +	*BINV	T-8
C_Intr (Sym)	6	C0: 7	TTL, +	*WARN	T-5
	5	C1: 5	TTL, +	*TRAP1	R-7
	4	C1: 6	TTL, +	*TRAP0	U-7

(Cont.)

Table C-4 (Cont.)
92DM72A Channel Assignments (C_Bus Module)

92DM72A Group (Radix)	Group Bit Pos	92A96 Section: Channel	Voltage Threshold, Polarity	Am29000/050 Signal Name	169-Pin PGA
C_Intr (Sym)	3	C1: 1	TTL, +	*INTR3	U-5
	2	C1: 2	TTL, +	*INTR2	T-6
	1	C1: 3	TTL, +	*INTR1	U-6
	0	C1: 4	TTL, +	*INTR0	T-7
C_Aux1 (Off)	3	C2: 4	TTL, +	*IBREQ‡§	U-8
	2	C1: 7	TTL, +	*IBACK‡§	U-4
	1	C0: 5	TTL, +	*PEN§	U-2
	0	C2: 6	TTL, +	*PIA§	U-10
C_Aux0 (Off)	9	C3: 6	TTL, +	MPGM1§	N-16
	8	C3: 7	TTL, +	MPGM0§	N-17
	7	C2: 5	TTL, +	STAT2§	R-12
	6	C3: 4	TTL, +	STAT1§	U-14
	5	C3: 1	TTL, +	STAT0§	T-13
	4	C0: 2	TTL, +	CNTL1§	P-1
	3	C0: 3	TTL, +	CNTL0§	P-2
	2	C3: 0	TTL, +	MSERR§	T-12
	1	C0: 1	TTL, +	*TEST§	N-2
	0	C1: 0	TTL, +	SYSCLK‡	N-3
Clock (not stored)	3	CLK: 3	TTL, +	*IBREQ‡	U-8
	2	CLK: 2	TTL, +	*IBACK‡	U-4
	1	CLK: 1	TTL, +	SYSCLK‡	N-3
	0	CLK: 0¶		none	none

† These signals are synthesized on the probe adapter.

‡ These signals are double probed.

§ These signals are not required for disassembly. Refer to Table B-4 to see how the disassembler uses them. Also refer to the *Hardware Analysis* section earlier in this manual for descriptions of sampling these signals asynchronously using Internal clocking.

¶This channel is not acquired or connected to the probe adapter.

Table C-5 shows the 92A96 section and channel assignments, their grouping and radix for the disassembler, the voltage threshold, polarity, and microprocessor signal and pin connections for the data module.

Table C-5
92DM72A Channel Assignments (D_Bus Module)

92DM72A Group (Radix)	Group Bit Pos	92A96 Section: Channel	Voltage Threshold, Polarity	Am29000/050 Signal Name	169-Pin PGA
D_Addr (Hex)	31	A3: 7	TTL, +	A31	D-15
	30	A3: 6	TTL, +	A30	B-17
	29	A3: 5	TTL, +	A29	C-17
	28	A3: 4	TTL, +	A28	D-16
	27	A3: 3	TTL, +	A27	E-16
	26	A3: 2	TTL, +	A26	D-17

(Cont.)

Table C-5 (Cont.)
92DM72A Channel Assignments (D_Bus Module)

92DM72A Group (Radix)	Group Bit Pos	92A96 Section: Channel	Voltage Threshold, Polarity	Am29000/050 Signal Name	169-Pin PGA
D_Addr (Cont.)	25	A3: 1	TTL, +	A25	F-15
	24	A3: 0	TTL, +	A24	F-16
	23	A2: 7	TTL, +	A23	E-17
	22	A2: 6	TTL, +	A22	G-15
	21	A2: 5	TTL, +	A21	F-17
	20	A2: 4	TTL, +	A20	G-16
	19	A2: 3	TTL, +	A19	G-17
	18	A2: 2	TTL, +	A18	H-16
	17	A2: 1	TTL, +	A17	H-17
	16	A2: 0	TTL, +	A16	J-16
	15	A1: 7	TTL, +	A15	J-15
	14	A1: 6	TTL, +	A14	J-17
	13	A1: 5	TTL, +	A13	K-17
	12	A1: 4	TTL, +	A12	K-16
	11	A1: 3	TTL, +	A11	L-17
	10	A1: 2	TTL, +	A10	L-16
	9	A1: 1	TTL, +	A9	P-17
	8	A1: 0	TTL, +	A8	P-16
	7	A0: 7	TTL, +	A7	R-17
	6	A0: 6	TTL, +	A6	R-16
	5	A0: 5	TTL, +	A5	P-15
	4	A0: 4	TTL, +	A4	T-17
	3	A0: 3	TTL, +	A3	T-16
	2	A0: 2	TTL, +	A2	R-15
	1	A0: 1	TTL, +	A1	M-17
	0	A0: 0	TTL, +	A0	M-16
D_Data (Hex)	31	D3: 7	TTL, +	D31	C-16
	30	D3: 6	TTL, +	D30	C-15
	29	D3: 5	TTL, +	D29	B-16
	28	D3: 4	TTL, +	D28	B-15
	27	D3: 3	TTL, +	D27	A-16
	26	D3: 2	TTL, +	D26	C-13
	25	D3: 1	TTL, +	D25	A-15
	24	D3: 0	TTL, +	D24	B-14
	23	D2: 7	TTL, +	D23	B-13
	22	D2: 6	TTL, +	D22	C-12
	21	D2: 5	TTL, +	D21	A-14
	20	D2: 4	TTL, +	D20	A-13
	19	D2: 3	TTL, +	D19	B-12
	18	D2 2	TTL, +	D18	A-12
	17	D2: 1	TTL, +	D17	B-11
	16	D2: 0	TTL, +	D16	A-11
	15	D1: 7	TTL, +	D15	B-10
	14	D1: 6	TTL, +	D14	A-10
	13	D1: 5	TTL, +	D13	B-9
	12	D1: 4	TTL, +	D12	A-9
	11	D1: 3	TTL, +	D11	A-8
	10	D1: 2	TTL, +	D10	B-8

(Cont.)

Table C-5 (Cont.)
92DM72A Channel Assignments (D_Bus Module)

92DM72A Group (Radix)	Group Bit Pos	92A96 Section: Channel	Voltage Threshold, Polarity	Am29000/050 Signal Name	169-Pin PGA
D_Data (Cont.)	9	D1: 1	TTL, +	D9	A-7
	8	D1: 0	TTL, +	D8	B-7
	7	D0: 7	TTL, +	D7	C-7
	6	D0: 6	TTL, +	D6	A-6
	5	D0: 5	TTL, +	D5	B-6
	4	D0: 4	TTL, +	D4	A-5
	3	D0: 3	TTL, +	D3	C-6
	2	D0: 2	TTL, +	D2	A-4
	1	D0: 1	TTL, +	D1	B-5
	0	D0: 0	TTL, +	D0	B-4
D_Ctrl (Sym)	12	C1: 2	TTL, +	B/*L†	none
	11	C2: 6	TTL, +	R/*W	U-11
	10	C1: 7	TTL, +	*BGRT‡	T-9
	9	C3: 1	TTL, +	DREQT1	U-12
	8	C3: 2	TTL, +	DREQT0	U-13
	7	C3: 7	TTL, +	OPT2	U-16
	6	C3: 6	TTL, +	OPT1	T-15
	5	C3: 5	TTL, +	OPT0	R-14
	4	C3: 3	TTL, +	SUP/*US	T-14
	3	C2: 5	TTL, +	*LOCK	T-11
	2	C1: 3	TTL, +	*RESET	R-1
	1	C2: 0	TTL, +	*DERR	T-3
	0	C2: 2	TTL, +	*BINV	T-8
D_Aux0 (Off)	8	C2: 7	TTL, +	*DREQ§	T-10
	7	C1: 1	TTL, +	*DRDY‡§	R-3
	6	C3: 0	TTL, +	*DBREQ‡§	R-9
	5	C2: 4	TTL, +	*DBACK‡§	R-4
	4	C3: 4	TTL, +	*PDA§	R-10
	3	C1: 5	TTL, +	*CDA§	R-2
	2	C1: 6	TTL, +	*BREQ§	T-2
	1	C2: 1	TTL, +	B-DREQ†	none
	0	C1: 0	TTL, +	SYSCLK‡	N-3
Clock (not stored)	3	CLK: 3	TTL, +	*DBREQ‡	R-9
	2	CLK: 2	TTL, +	*BGRT‡	T-9
	1	CLK: 1	TTL, +	*DRDY‡	R-3
	0	CLK: 0		SYSCLK‡	N-3

† These signals are synthesized on the probe adapter.

‡ These signals are double probed.

§ These signals are not required for disassembly. Refer to Table B-4 to see how the disassembler uses them. Also refer to the *Hardware Analysis* section earlier in this manual for descriptions of sampling these signals asynchronously using Internal clocking.

Figure C-1 shows the dimensions of and minimum clearances for the probe adapter with all the clock probes and 8-channel probes attached.

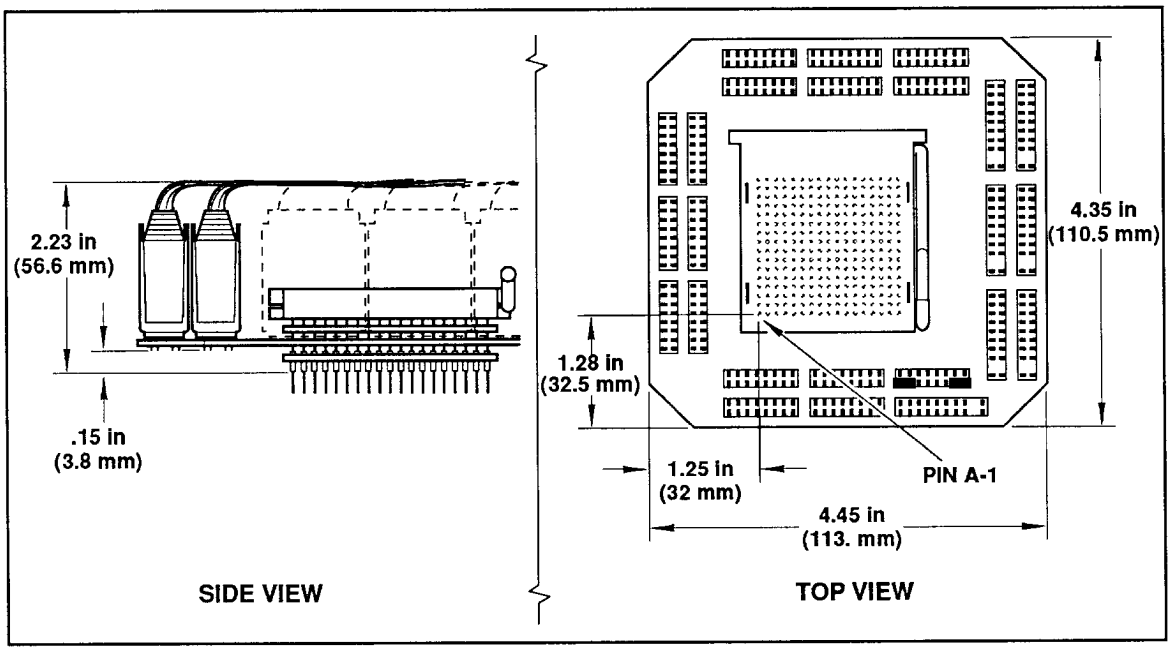


Figure C-1. Dimensions of and minimum clearances for the probe adapter with 8-channel probes attached.

DISCONNECTING CLOCK AND 8-CHANNEL PROBES

You may need to disconnect the clock and 8-channel probes from the probe adapter to do the following:

- to use the 92A96 Module with another application
- to connect individual channels from an 8-channel probe (podlets) to other signals in your Am29000/050 system
- to replace defective clock or 8-channel probe podlets

Refer to Figure C-2 and the following procedure to disconnect the clock and 8-channel probes from the probe adapter. Use the antistatic shipping material to support the probe adapter while disconnecting the probes.

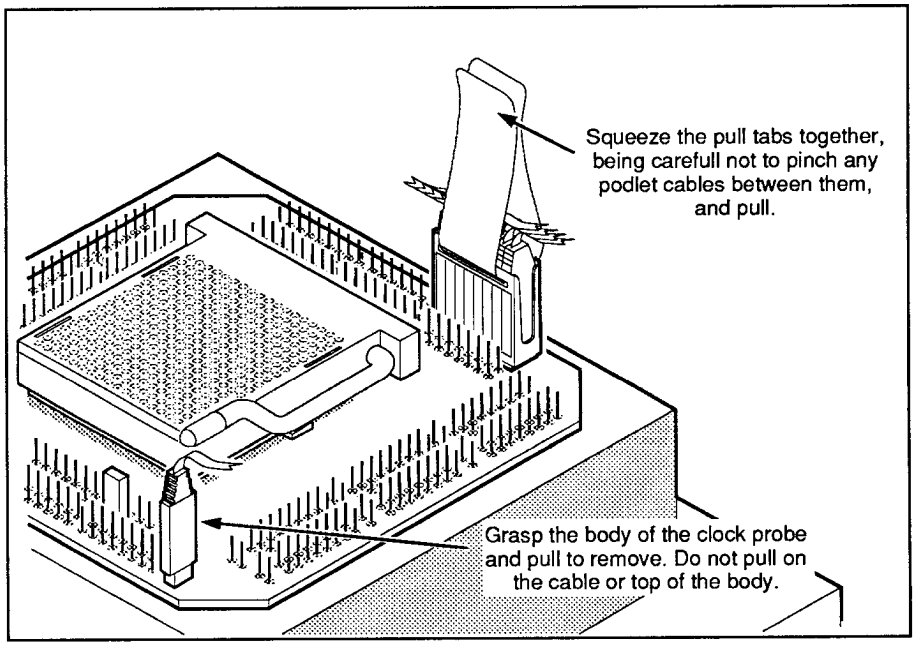


Figure C-2. Disconnecting clock and 8-channel probes from the probe adapter.

1. Power down the Am29000/050 system. It is not necessary to power down the DAS 9200.
2. Steady the probe adapter to prevent it from teetering when disconnecting a clock or 8-channel probe.

CAUTION

You can can damage the 8-channel probes by pulling on the cables or pinching the cables between the pull tabs. You can damage the clock probe by pulling on the neck of the body. Always remove the probes by their bodies or the pull tabs.

3. Firmly grasp the body of a clock probe and gently pull it off the square pins.
4. Squeeze the pull tabs on the podlet holder together, and be careful not to pinch any podlet cables between them.
5. Gently pull the 8-channel probe off the square pins.

REMOVING AND REPLACING PODLETS

Each 8-channel probe consists of 8 single-channel podlets ganged together in a podlet holder. You may need to remove these podlets from the 8-channel probe to use for alternate connections to Am29000/050 system signals.

Refer to the discussions on *Signals* in Appendix A and *Alternate Connections* in Section 3 for information on which channels you can use to make alternate connections between the DAS 9200 and system under test without disturbing the channel connections required for disassembly.

You can also use these procedures to replace a defective clock probe or a defective podlet from an 8-channel probe.

Removing a Clock Probe or 8-Channel Probe Podlet from the Interface Housing

Refer to Figure C-3 and the following procedure to remove a clock probe or an 8-channel probe podlet from the interface housing.

1. Power down the SUT. It is not necessary to power down the DAS 9200.
2. Use a small pointed tool such as a ballpoint pen, pencil, or straightened paper clip to press down on the latch detent of the podlet through an opening on the interface housing.
3. Gently pull the podlet connector out of the housing with one hand while pressing down on the latch detent with the pointed tool.

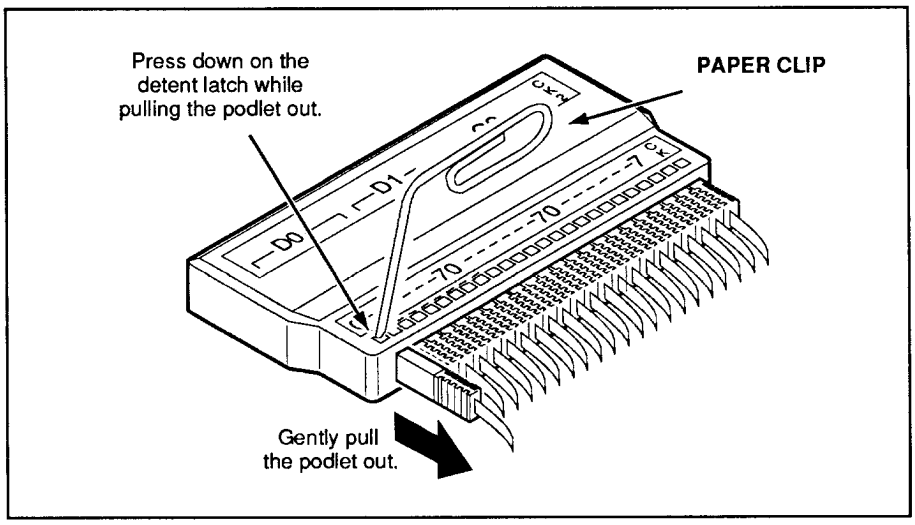


Figure C-3. Removing a clock or an 8-channel probe podlet from the interface housing.

Replacing a Clock Probe

To replace a clock probe, insert a new clock probe into the same clock channel position on the interface housing. Insert the clock probe into the interface housing with the detent latch oriented to the label side of the housing. Refer to Figure C-3.

Removing 8-Channel Probe Podlets from the Podlet Holder

Refer to Figure C-4 and the following procedure to remove the 8-channel probe podlets from the podlet holder.

CAUTION

Spread the podlet holder open wide enough to clear and remove the podlets. Excessive pulling on the sides of the podlet holder can break it.

1. To remove podlets from the podlet holder, grasp the plastic pull tab on each side of the podlet holder and gently spread the sides of the holder open just enough to clear a podlet.
2. Remove the middle two podlets from the podlet holder by pushing up on the metal pin receptacles.
3. Release the tabs on the podlet holder.
4. Remove the remaining podlets by turning and extracting one at a time.

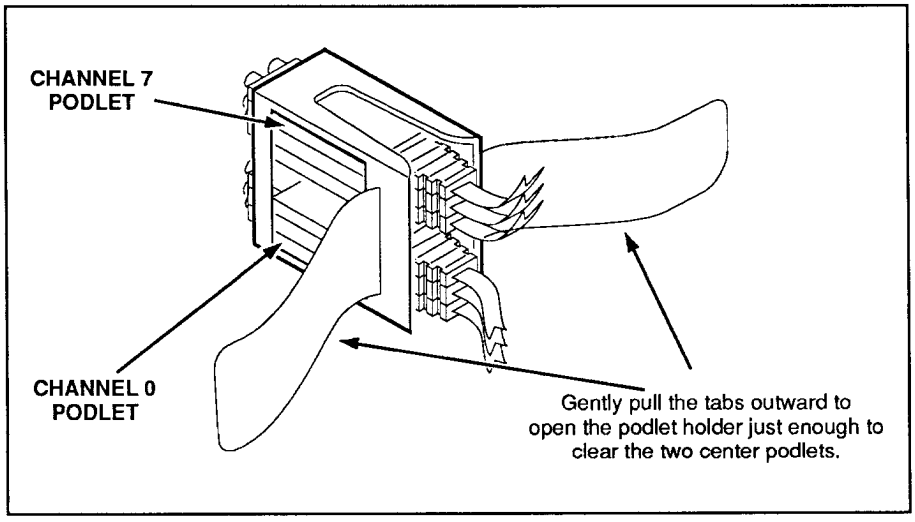


Figure C-4. Ganging the 8-channel probe podlets together.

Replacing 8-Channel Probe Podlets

The channel podlets must retain the same channel order on both the interface housing and in the podlet holder. Be sure to replace the old podlet with a podlet of the same color. Table C-6 shows the color code and channel number of each podlet for an 8-channel probe.

Table C-6
Podlet-to-Channel Color Code

Podlet Color	Channel
Black	0
Brown	1
Red	2
Orange	3
Yellow	4
Green	5
Blue	6
Violet	7

Refer to Figure C-4 and the following procedure to replace an 8-channel probe podlet.

1. Insert the appropriately colored podlet into the interface housing with the detent latch oriented to the label side of the housing.
2. If you are replacing a single podlet, orient the podlet channel marked GND towards the side of the podlet holder labeled GROUND.
3. Grasp the plastic pull tab on each side of the holder and gently spread the sides of the holder open just enough to clear the podlet.
4. Hold the podlet body with the other hand and place it in the holder in the correct channel order. Do not grasp and turn the podlet cable.
5. If you are re-ganging all the podlets of an 8-channel probe, begin ganging the podlets together starting with either channel 0 or channel 7. Orient the podlet channel marked GND towards the side of the podlet holder labeled GROUND.

CAUTION

To prevent damage to the podlets, keep the podlet cables parallel to each other when ganging them into the holder. Avoid twisting the podlet cables between the interface housing and the podlet holder.

6. Hold the podlet body, turn the podlet body parallel to the sides of the holder, move it into the holder, and use your fingers to press it into place perpendicular to the sides of the holder. Be sure to gang the podlets in the correct channel order according to the channel label on the podlet holder and podlet color code, with all ground channels toward the Ground side of the holder. Do not place the podlet into the holder by grasping the podlet cable.

7. Continue placing the next two podlets, one at a time, in channel order, in the podlet holder. Orient all ground channels toward the Ground side of the holder.
8. The fourth podlet should be either channel 0 or 7, whichever one is not already placed in the holder. Place this podlet in the other end of the podlet holder. Orient the ground channel correctly.
9. Continue placing the next two podlets, one at a time, in channel order, in the podlet holder. Continue orienting the ground channels correctly.

CAUTION

Spread the podlet holder open wide enough to clear the podlet. Excessive pulling on the sides of the podlet holder can break it.

10. Grasp the plastic pull tab on each side of the holder and gently spread the sides of the holder open just enough to clear a podlet.
11. Place the last pair of podlets (channels 3 and 4) in the podlet holder in proper channel order, orienting the ground channels to the Ground side of the holder.

REMOVING AND REPLACING SOCKETS

The probe adapter board contains several sockets designed to protect the probe adapter and to make it easy to insert and remove the Am29000/050 microprocessor. Figure C-5 shows a side view of the board, sockets, and pins of the probe adapter. The fixed socket on top of the probe adapter board is soldered and cannot be removed. The following paragraphs describe how to remove and replace the ZIF socket and the protective socket on the bottom of the probe adapter board.

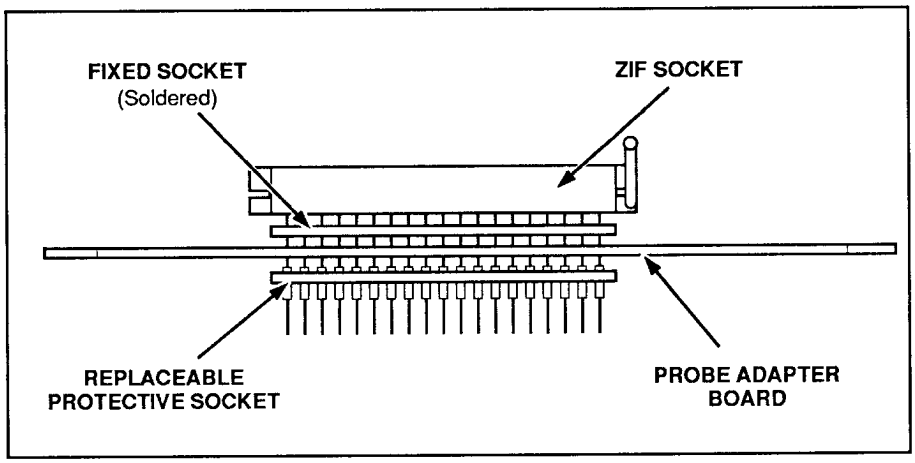


Figure C-5. Side view of the probe adapter board.

ZIF Socket

You should not have to remove the ZIF socket unless there are clearance problems or socket-pin damage. To remove the ZIF socket, refer to Figure C-5 and follow these steps:

1. Place a 3/16" flat-blade screwdriver between the fixed socket and the ZIF socket. The screwdriver should rest on the top of the body of the fixed socket.

CAUTION

Do not pry off one side of the ZIF socket and then the other. Applying uneven pressure can damage the ZIF socket's pins. Apply even pressure around the entire socket.

2. Gently twist the screwdriver against the body of the fixed socket and the ZIF socket until the ZIF socket is loose.
3. Remove the ZIF socket from the board.
4. Once the ZIF socket has been removed from the board, store the ZIF socket in protective foam so that the pins are not damaged.

To replace the ZIF socket, follow these steps:

1. Check that the ZIF socket's pins are straight.
2. Refer to Figure 2-8 for pin A1 location information.
3. After locating the correct pin A1 location for the 92DM72A, align the ZIF socket with the fixed socket on the board, making sure that all pins line up correctly.
4. Apply even pressure on the ZIF socket, so that all pins insert evenly.

Replaceable Protective Socket

You should not have to remove the probe adapter's replaceable protective socket unless there is socket-pin damage. To remove the protective socket, refer to Figure C-5 and follow these steps:

1. Locate the side of the socket adjacent to the edge of the probe adapter board and the side of the socket labeled A through S.

CAUTION

Be careful not to damage any etched circuit board runs or components surrounding the protective socket when using a screwdriver to remove the protective socket from the bottom of the probe adapter board.

2. Place a 3/16" flat-blade screwdriver between the socket and the board on the side adjacent to the edge of the probe adapter board.

CAUTION

Do not completely pry off one side of the protective socket and then the other. Applying uneven pressure can damage the socket's pins. Do not use board components as leverage to remove the socket.

3. Gently twist the screwdriver against the body of the socket until the socket begins to separate from the probe adapter board pins.
4. Twist the screwdriver against the body of the socket next to the board marked A through S, but only where there are no board runs. Use even pressure alternately on both sides of the socket until the socket is loose.
5. Remove the socket from the board.

To replace the protective socket, follow these steps:

1. Check that the new socket's pins are straight.
2. Place the socket on the pins of the probe adapter board; make sure that all pins line up correctly.
3. Press the socket onto the board by pressing the socket and board against a hard, flat surface while applying even pressure.

Replaceable Electrical Parts

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

LIST OF ASSEMBLIES

A list of assemblies can be found at the beginning of the Electrical Parts List. The assemblies are listed in numerical order. When the complete component number of a part is known, this list will identify the assembly in which the part is located.

CROSS INDEX-MFR. CODE NUMBER TO MANUFACTURER

The Mfr. Code Number to Manufacturer index for the Electrical Parts List is located immediately after this page. The Cross Index provides codes, names and addresses of manufacturers of components listed in the Electrical Parts List.

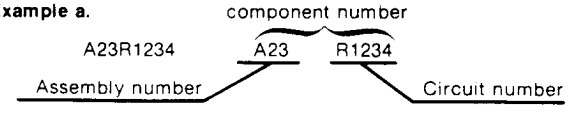
ABBREVIATIONS

Abbreviations conform to American National Standard Y1.1.

COMPONENT NUMBER (column one of the Electrical Parts List)

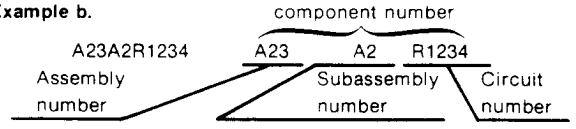
A numbering method has been used to identify assemblies, subassemblies and parts. Examples of this numbering method and typical expansions are illustrated by the following:

Example a.



Read: Resistor 1234 of Assembly 23

Example b.



Read: Resistor 1234 of Subassembly 2 of Assembly 23

Only the circuit number will appear on the diagrams and circuit board illustrations. Each diagram and circuit board illustration is clearly marked with the assembly number. Assembly numbers are also marked on the mechanical exploded views located in the Mechanical Parts List. The component number is obtained by adding the assembly number prefix to the circuit number.

The Electrical Parts List is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly A2 with its subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the Electrical Parts List.

TEKTRONIX PART NO. (column two of the Electrical Parts List)

Indicates part number to be used when ordering replacement part from Tektronix.

SERIAL/MODEL NO. (columns three and four of the Electrical Parts List)

Column three (3) indicates the serial number at which the part was first used. Column four (4) indicates the serial number at which the part was removed. No serial number entered indicates part is good for all serial numbers.

NAME & DESCRIPTION (column five of the Electrical Parts List)

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

MFR. CODE (column six of the Electrical Parts List)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

MFR. PART NUMBER (column seven of the Electrical Parts List)

Indicates actual manufacturers part number.

CROSS INDEX – MFR CODE NUMBER TO MANUFACTURER

Mfr Code	Manufacturer	Address	City, State, Zip Code
04222	AVX CERAMICS DIV OF AVX CORP	19TH AVE SOUTH P O BOX 867	MYRTLE BEACH SC 29577
04713	MOTOROLA INC	5005 E MCDOWELL RD	PHOENIX AZ 85008-4229
18324	SIGNETICS CORP	4130 S MARKET COURT	SACRAMENTO CA 95834-1222
22526	DU PONT E I DE NEMOURS AND CO INC	515 FISHING CREEK RD	NEW CUMBERLAND PA 17070-3007
53387	MINNESOTA MINING MFG CO	PO BOX 2963	AUSTIN TX 78769-2963
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR	BEAVERTON OR 97077-0001

REPLACEABLE ELECTRICAL PARTS

Component No.	Tektronix Part Number	Serial Number Effect	Serial Number Discont	Part Name & Description	Mfr Code	Mfr Part Number
A1	671-1977-00			CIRCUIT BD ASSY:92DM72 29000 PROBE ADAPTER	80009	671-1977-00
A1C310	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A1C320	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A1C411	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A1C510	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A1C710	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A1C720	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A1J210	131-5267-00			TERMINAL PIN:0.345 L X 0.100,0.025 SQ,GOLD	53387	DHY-2072-001A10-57E
A1J211	131-5267-00			TERMINAL PIN:0.345 L X 0.100,0.025 SQ,GOLD	53387	DHY-2072-001A10-57E
A1J220	131-5267-00			TERMINAL PIN:0.345 L X 0.100,0.025 SQ,GOLD	53387	DHY-2072-001A10-57E
A1J300	131-5267-00			TERMINAL PIN:0.345 L X 0.100,0.025 SQ,GOLD	53387	DHY-2072-001A10-57E
A1J301	131-5267-00			TERMINAL PIN:0.345 L X 0.100,0.025 SQ,GOLD	53387	DHY-2072-001A10-57E
A1J310	131-5267-00			TERMINAL PIN:0.345 L X 0.100,0.025 SQ,GOLD	53387	DHY-2072-001A10-57E
A1J311	131-5267-00			TERMINAL PIN:0.345 L X 0.100,0.025 SQ,GOLD	53387	DHY-2072-001A10-57E
A1J320	131-5267-00			TERMINAL PIN:0.345 L X 0.100,0.025 SQ,GOLD	53387	DHY-2072-001A10-57E
A1J400	131-5267-00			TERMINAL PIN:0.345 L X 0.100,0.025 SQ,GOLD	53387	DHY-2072-001A10-57E
A1J401	131-5267-00			TERMINAL PIN:0.345 L X 0.100,0.025 SQ,GOLD	53387	DHY-2072-001A10-57E
A1J420	131-5267-00			TERMINAL PIN:0.345 L X 0.100,0.025 SQ,GOLD	53387	DHY-2072-001A10-57E
A1J421	131-5267-00			TERMINAL PIN:0.345 L X 0.100,0.025 SQ,GOLD	53387	DHY-2072-001A10-57E
A1J520	131-5267-00			TERMINAL PIN:0.345 L X 0.100,0.025 SQ,GOLD	53387	DHY-2072-001A10-57E
A1J521	131-5267-00			TERMINAL PIN:0.345 L X 0.100,0.025 SQ,GOLD	53387	DHY-2072-001A10-57E
A1J600	131-5267-00			TERMINAL PIN:0.345 L X 0.100,0.025 SQ,GOLD	53387	DHY-2072-001A10-57E
A1J601	131-5267-00			TERMINAL PIN:0.345 L X 0.100,0.025 SQ,GOLD	53387	DHY-2072-001A10-57E
A1J700	131-5267-00			TERMINAL PIN:0.345 L X 0.100,0.025 SQ,GOLD	53387	DHY-2072-001A10-57E
A1J710	131-5267-00			TERMINAL PIN:0.345 L X 0.100,0.025 SQ,GOLD	53387	DHY-2072-001A10-57E
A1J720	131-5267-00			TERMINAL PIN:0.345 L X 0.100,0.025 SQ,GOLD	53387	DHY-2072-001A10-57E
A1J721	131-5267-00			TERMINAL PIN:0.345 L X 0.100,0.025 SQ,GOLD	53387	DHY-2072-001A10-57E
A1J722	131-5267-00			TERMINAL PIN:0.345 L X 0.100,0.025 SQ,GOLD	53387	DHY-2072-001A10-57E
A1J800	131-5267-00			TERMINAL PIN:0.345 L X 0.100,0.025 SQ,GOLD	53387	DHY-2072-001A10-57E
A1J810	131-5267-00			TERMINAL PIN:0.345 L X 0.100,0.025 SQ,GOLD	53387	DHY-2072-001A10-57E
A1J820	131-5267-00			TERMINAL PIN:0.345 L X 0.100,0.025 SQ,GOLD	53387	DHY-2072-001A10-57E
A1P601	131-3199-00			BUS,CONDUCTOR:SHUNT,1 X 2,0.1 CTR,JUMPER	22526	68786-202
A1U411	156-5514-00			IC,DIGITAL:FTTL,FLIP FLOP:OCTAL D-TYPE,	18324	74F377
A1U710	156-5051-00			IC,DIGITAL:FTTL,GATE:QUAD 2-INPUT NOR;74F02	04713	74F02
A1U720	156-5167-00			IC,DIGITAL:FTTL,COUNTER;8-BIT BIDIRECTIONAL	18324	N74F269D

DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS

SYMBOLS

Graphic symbol and class designation letters are based on ANSI Y32.14, 1973 in terms of positive logic. Logic symbols are depicted according to the manufacturer's data book information (not according to function).

Letter symbols for quantities used in electrical science and electrical engineering are based on ANSI Y10.5, 1968.

Drafting practices, line conventions, and lettering conform to ANSI Y14.15, 1966 and ANSI Y14.2, 1973.

Abbreviations are based on ANSI Y1.1, 1972.

You can inquire about these ANSI standards by contacting:

American National Standard Institute
1430 Broadway
New York, New York 10018

COMPONENT VALUES

Electrical components shown on the diagram are in the following units unless noted otherwise:

Capacitors = Values one or greater are in picofarads(pF)
Values less then one are in microfarads (μF)

Resistors = Ohms (Ω)

ACTIVE-LOW SIGNAL INDICATORS

A common convention used for indicating an active-low signal (a signal performing its intended function when it is in a low state) is an overbar, as shown in the signal name $\overline{\text{RESET}}$. The overbar may be used in this manual whenever a reference is given to an active-low signal. However, the same active-low signal is indicated on the schematic with a tilde (~), or a slash (/) following the signal name (e.g., RESET~ or RESET/).

The information and special symbols below may appear in this manual.

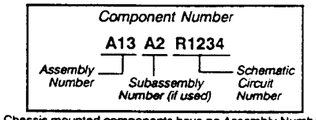
ASSEMBLY NUMBERS

Each assembly in the instrument is assigned an assembly number (e.g., A5). The assembly number appears in the title of each:

- schematic diagram (lower right corner)
- circuit board component location illustration
- schematic or circuit board component location look up table (when shown).

The Replaceable Electrical Parts list is arranged by assemblies in numerical order. The components are listed alphabetically by component location numbers. Look at the following example to see how to construct a component number.

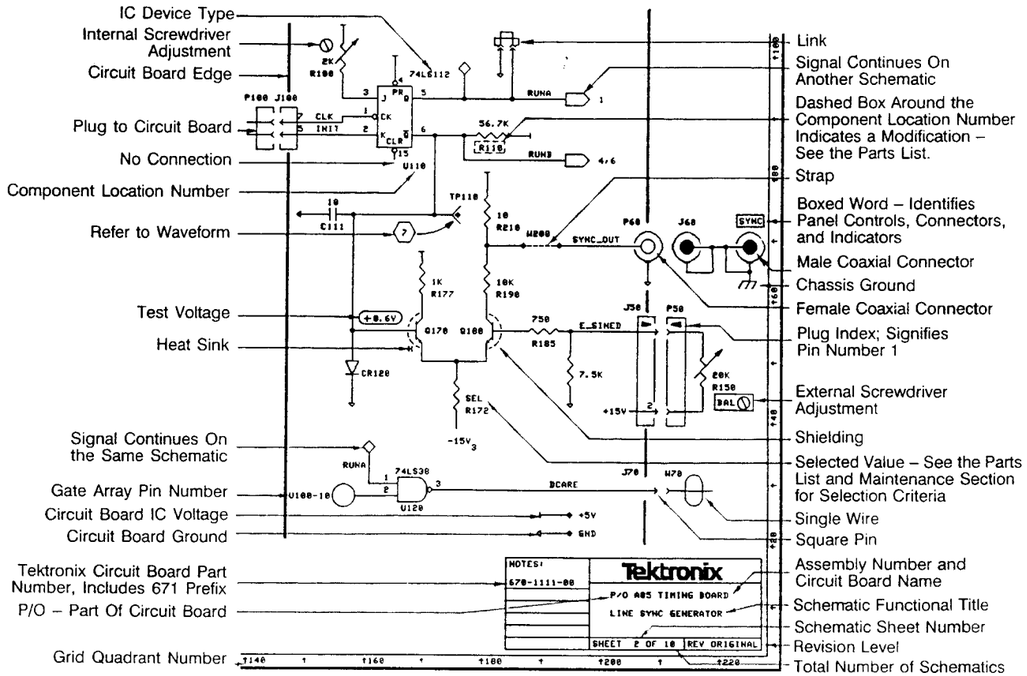
COMPONENT NUMBER EXAMPLE

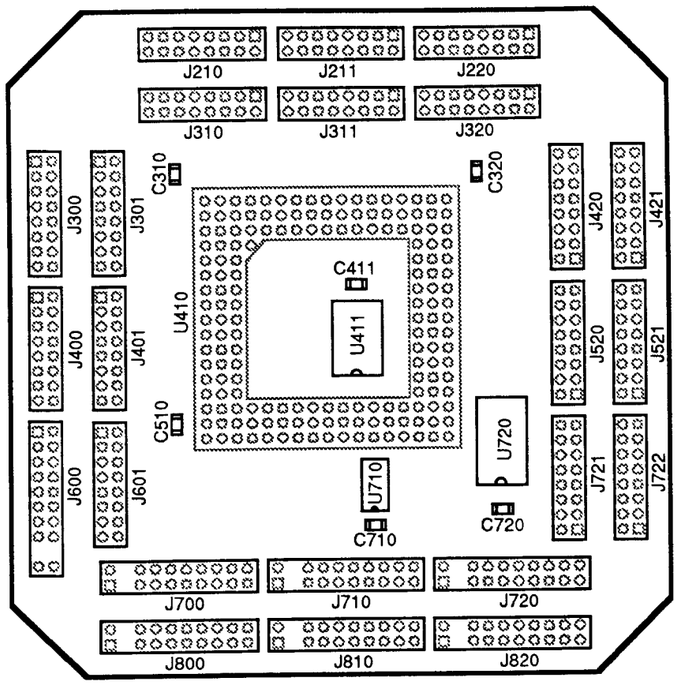


Chassis mounted components have no Assembly Number prefix – see end of Replaceable Parts List.

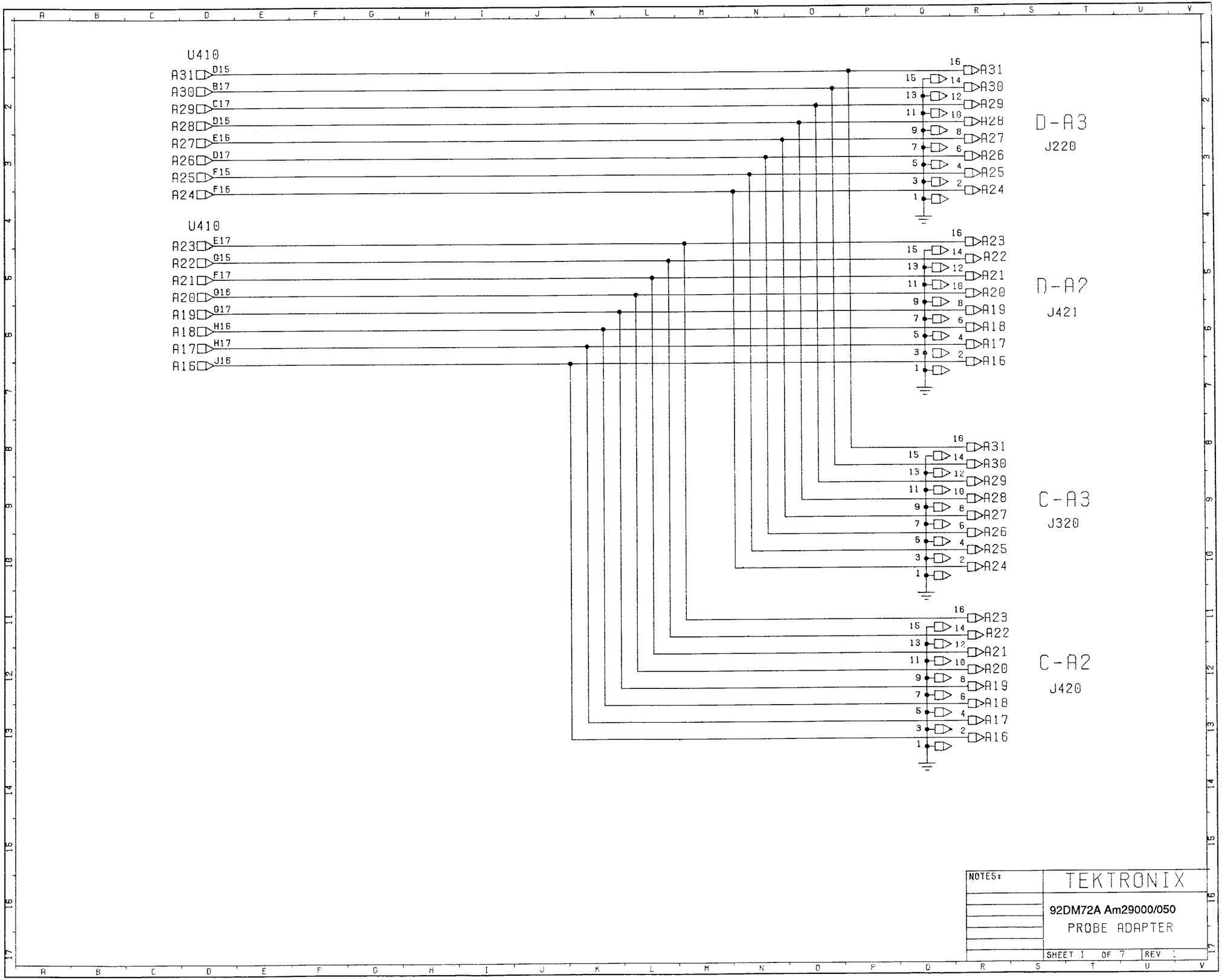
GRID COORDINATES

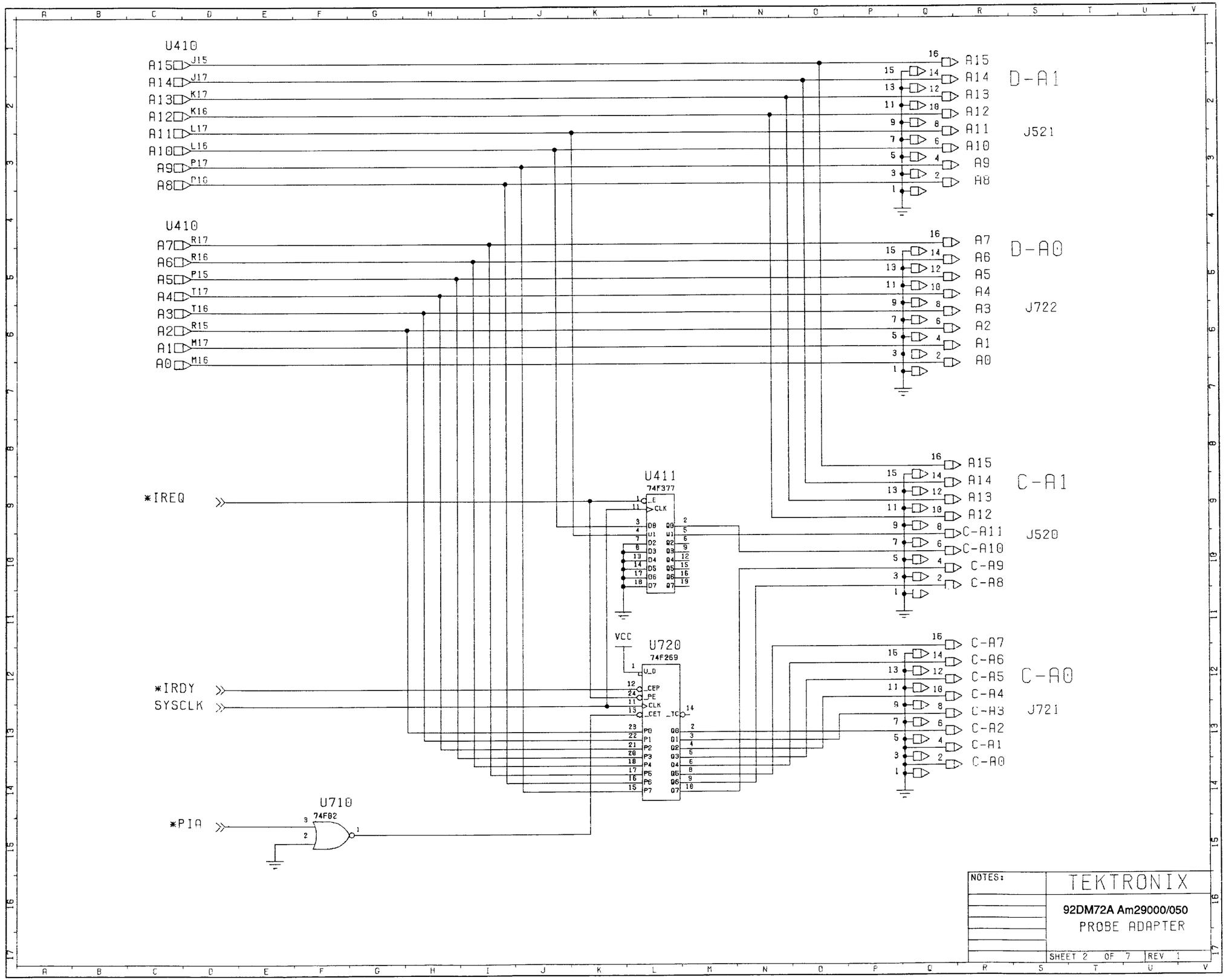
The schematic diagram(s) and circuit board component location illustration both have grids. A look up table (when shown) provides grid coordinates for ease of locating components. There may be two tables for each assembly: one for the circuit board component location illustration and one for the schematic diagram(s).





92DM72A Probe Adapter board component locations.


U410
A31 D15
A30 B17
A29 C17
A28 D16
A27 E16
A26 D17
A25 F15
A24 F16
U410
A23 E17
A22 G15
A21 F17
A20 G16
A19 G17
A18 H16
A17 H17
A16 J16
16 A31
15 14 A30
13 12 A29
11 10 A28
9 8 A27
7 6 A26
5 4 A25
3 2 A24
1
D-A3
J220
16 A23
15 14 A22
13 12 A21
11 10 A20
9 8 A19
7 6 A18
5 4 A17
3 2 A16
1
D-A2
J421
16 A31
15 14 A30
13 12 A29
11 10 A28
9 8 A27
7 6 A26
5 4 A25
3 2 A24
1
C-A3
J320
16 A23
15 14 A22
13 12 A21
11 10 A20
9 8 A19
7 6 A18
5 4 A17
3 2 A16
1
C-A2
J420
NOTES:
TEKTRONIX
92DM72A Am29000/050
PROBE ADAPTER
SHEET 1 OF 7
REV :


U410
A15
A14
A13
A12
A11
A10
A9
A8
J15
J17
K17
K16
L17
L16
P17
P16
U410
A7
A6
A5
A4
A3
A2
A1
A0
R17
R16
P15
T17
T16
R15
M17
M16
U411
74F377
*IREQ
*IRDY
SYSCLK
VCC
U720
74F269
U710
74F02
*PIA
D-A1
J521
D-A0
J722
C-A1
J520
C-A0
J721
TEKTRONIX
92DM72A Am29000/050
PROBE ADAPTER
NOTES:
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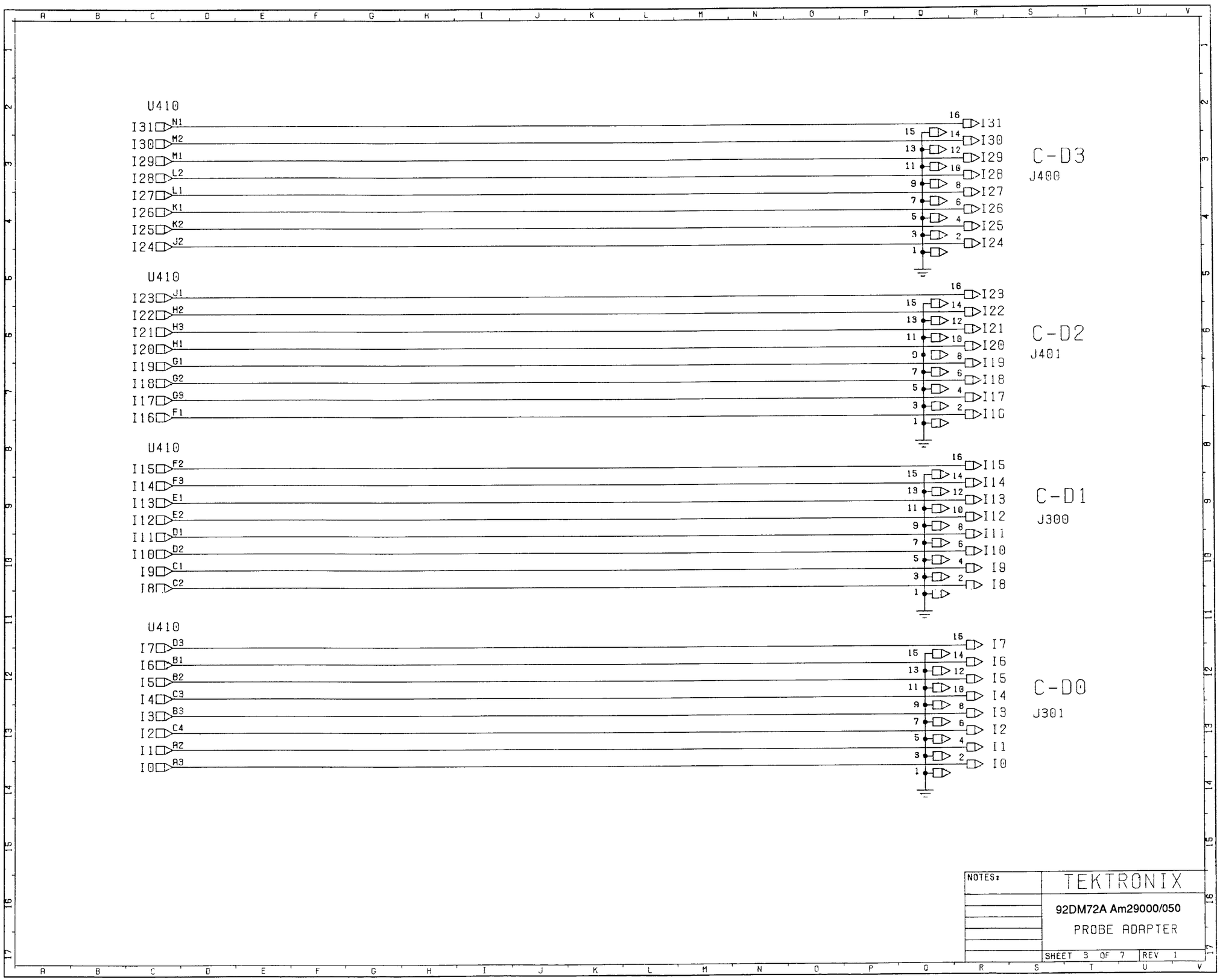
U410
I31 N1
I30 M2
I29 M1
I28 L2
I27 L1
I26 K1
I25 K2
I24 J2
16 I31
15 14 I30
13 12 I29
11 10 I28
9 8 I27
7 6 I26
5 4 I25
3 2 I24
1
C-D3
J400
U410
I23 J1
I22 H2
I21 H3
I20 H1
I19 G1
I18 G2
I17 G3
I16 F1
16 I23
15 14 I22
13 12 I21
11 10 I20
9 8 I19
7 6 I18
5 4 I17
3 2 I16
1
C-D2
J401
U410
I15 F2
I14 F3
I13 E1
I12 E2
I11 D1
I10 D2
I9 C1
I8 C2
16 I15
15 14 I14
13 12 I13
11 10 I12
9 8 I11
7 6 I10
5 4 I9
3 2 I8
1
C-D1
J300
U410
I7 D3
I6 B1
I5 B2
I4 C3
I3 B3
I2 C4
I1 A2
I0 A3
16 I7
15 14 I6
13 12 I5
11 10 I4
9 8 I3
7 6 I2
5 4 I1
3 2 I0
1
C-D0
J301
NOTES:
TEKTRONIX
92DM72A Am29000/050
PROBE ADAPTER
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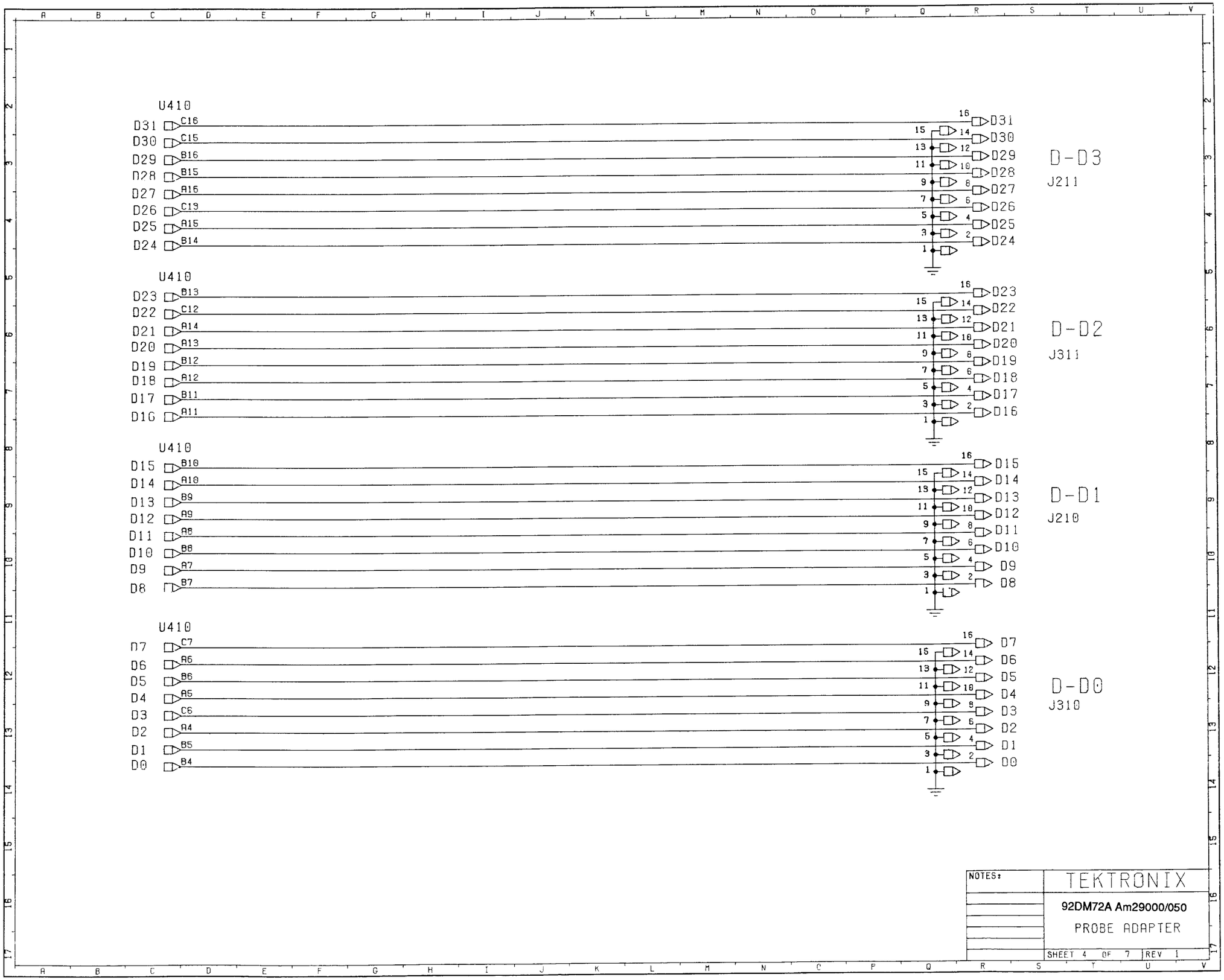
U410
D31 C16
D30 C15
D29 B16
D28 B15
D27 A16
D26 C13
D25 A15
D24 B14
16 D31
15 14 D30
13 12 D29
11 10 D28
9 8 D27
7 6 D26
5 4 D25
3 2 D24
1
D-D3
J211
U410
D23 B13
D22 C12
D21 A14
D20 A13
D19 B12
D18 A12
D17 B11
D16 A11
16 D23
15 14 D22
13 12 D21
11 10 D20
9 8 D19
7 6 D18
5 4 D17
3 2 D16
1
D-D2
J311
U410
D15 B10
D14 A10
D13 B9
D12 A9
D11 A8
D10 B8
D9 A7
D8 B7
16 D15
15 14 D14
13 12 D13
11 10 D12
9 8 D11
7 6 D10
5 4 D9
3 2 D8
1
D-D1
J210
U410
D7 C7
D6 A6
D5 B6
D4 A5
D3 C6
D2 A4
D1 B5
D0 B4
16 D7
15 14 D6
13 12 D5
11 10 D4
9 8 D3
7 6 D2
5 4 D1
3 2 D0
1
D-D0
J310
NOTES:
TEKTRONIX
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PROBE ADAPTER
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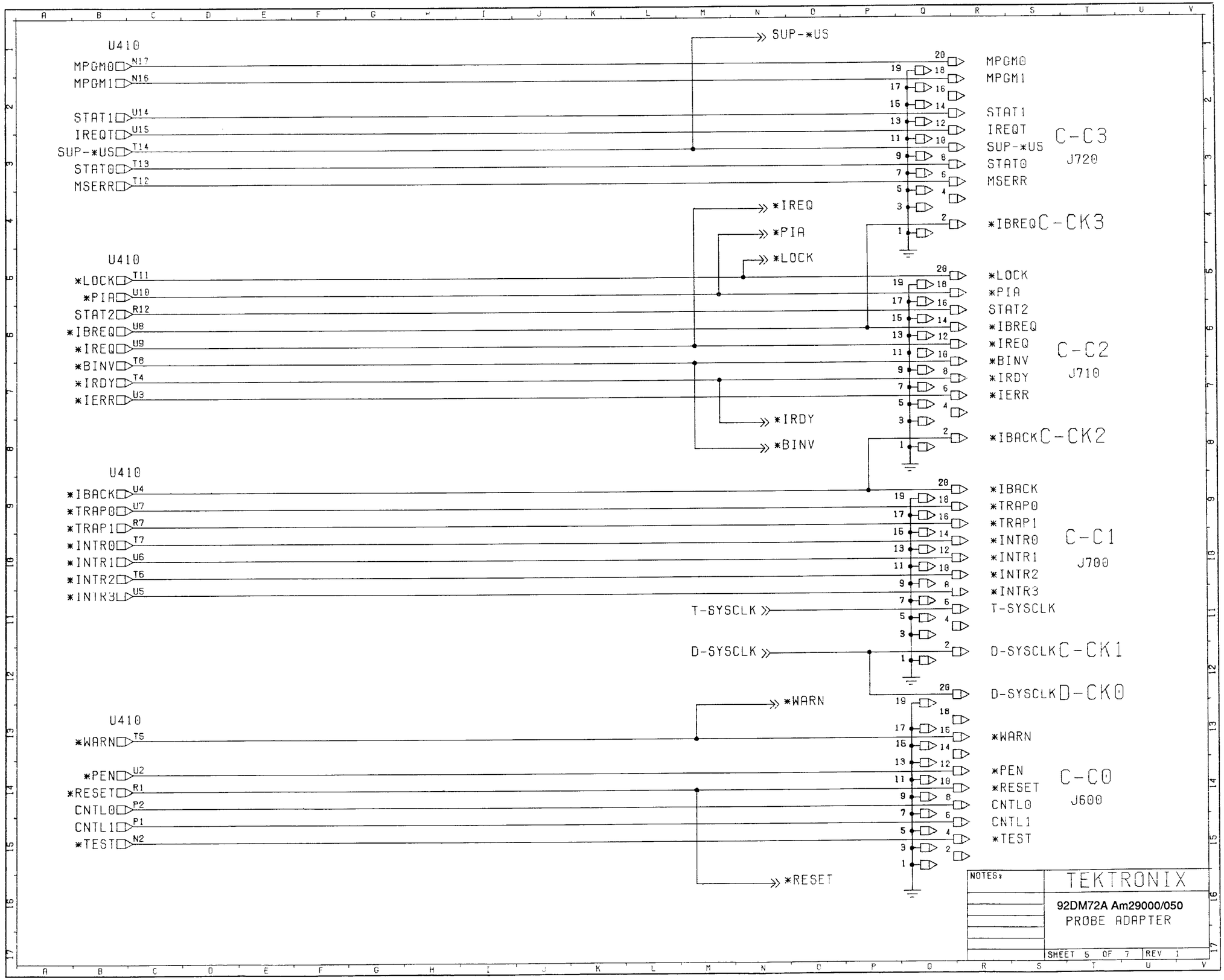
U410
MPGM0 N17
MPGM1 N16
STAT1 U14
IREQT U15
SUP-*US T14
STAT0 T13
MSERR T12
SUP-*US
*IREQ
*PIA
*LOCK
*IRDY
*BINV
MPGM0
MPGM1
STAT1
IREQT
SUP-*US
STAT0
MSERR
C-C3
J720
*IBREQ C-CK3
U410
*LOCK T11
*PIA U10
STAT2 R12
*IBREQ U8
*IREQ U9
*BINV T8
*IRDY T4
*IERR U3
*LOCK
*PIA
STAT2
*IBREQ
*IREQ
*BINV
*IRDY
*IERR
C-C2
J710
*IBACK C-CK2
U410
*IBACK U4
*TRAP0 U7
*TRAP1 R7
*INTR0 T7
*INTR1 U6
*INTR2 T6
*INTR3 U5
T-SYSCLK
*IBACK
*TRAP0
*TRAP1
*INTR0
*INTR1
*INTR2
*INTR3
T-SYSCLK
C-C1
J700
D-SYSCLK C-CK1
D-SYSCLK D-CK0
U410
*WARN T5
*PEN U2
*RESET R1
CNTL0 P2
CNTL1 P1
*TEST N2
*WARN
*RESET
*WARN
*PEN
*RESET
CNTL0
CNTL1
*TEST
C-C0
J600
NOTES:
TEKTRONIX
92DM72A Am29000/050
PROBE ADAPTER
SHEET 5 OF 7
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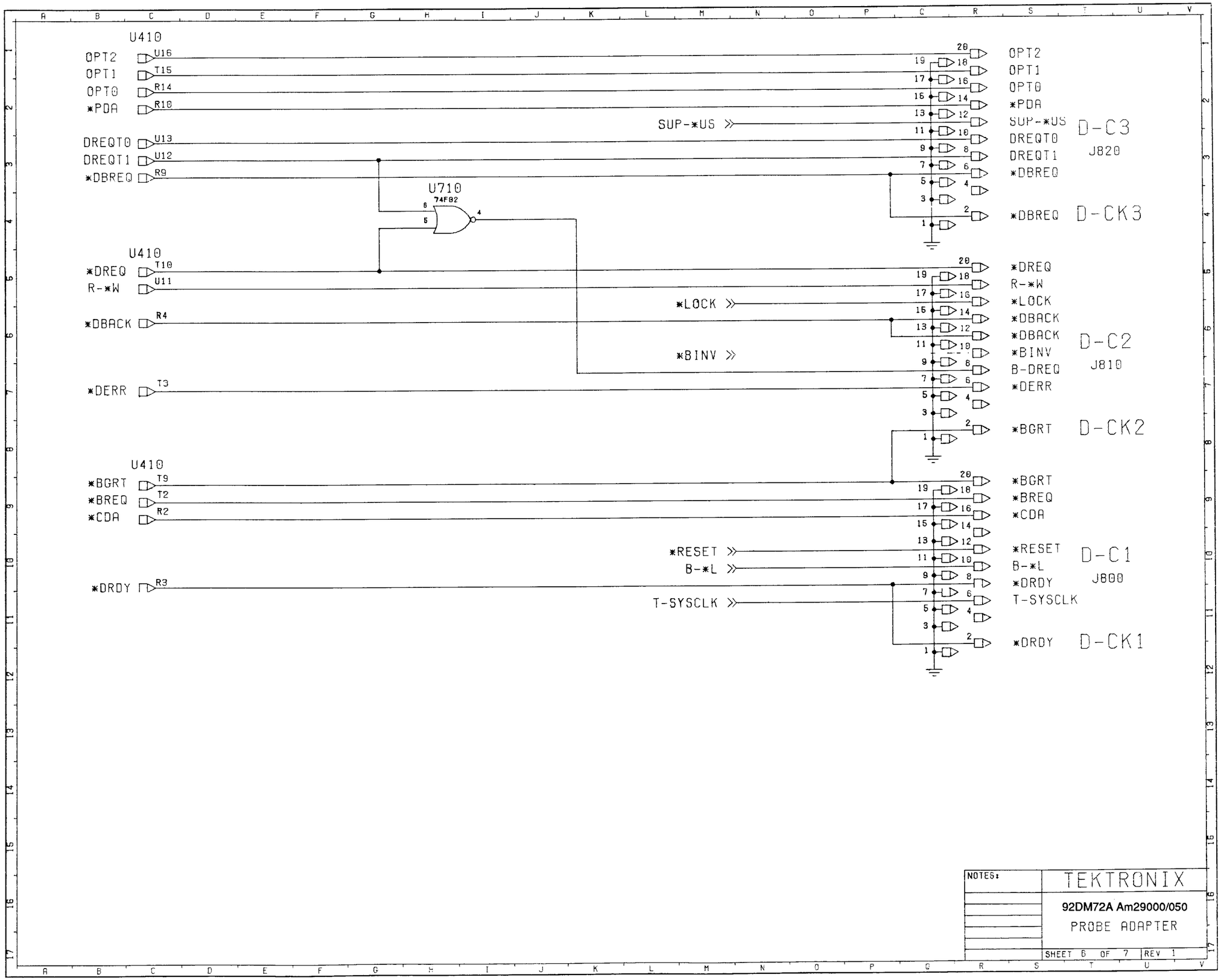
U410
OPT2 U16
OPT1 T15
OPT0 R14
*PDA R10
DREQT0 U13
DREQT1 U12
*DBREQ R9
U710
74F02
U410
*DREQ T10
R-*W U11
*DBACK R4
*DERR T3
U410
*BGRT T9
*BREQ T2
*CDA R2
*DRDY R3
SUP-*US »
*LOCK »
*BINV »
*RESET »
B-*L »
T-SYSCLK »
OPT2
OPT1
OPT0
*PDA
SUP-*US
DREQT0
DREQT1
*DBREQ
D-C3
J820
*DBREQ
D-CK3
*DREQ
R-*W
*LOCK
*DBACK
*DBACK
*BINV
B-DREQ
*DERR
D-C2
J810
*BGRT
D-CK2
*BGRT
*BREQ
*CDA
*RESET
B-*L
*DRDY
T-SYSCLK
D-C1
J800
*DRDY
D-CK1
NOTES:
TEKTRONIX
92DM72A Am29000/050
PROBE ADAPTER
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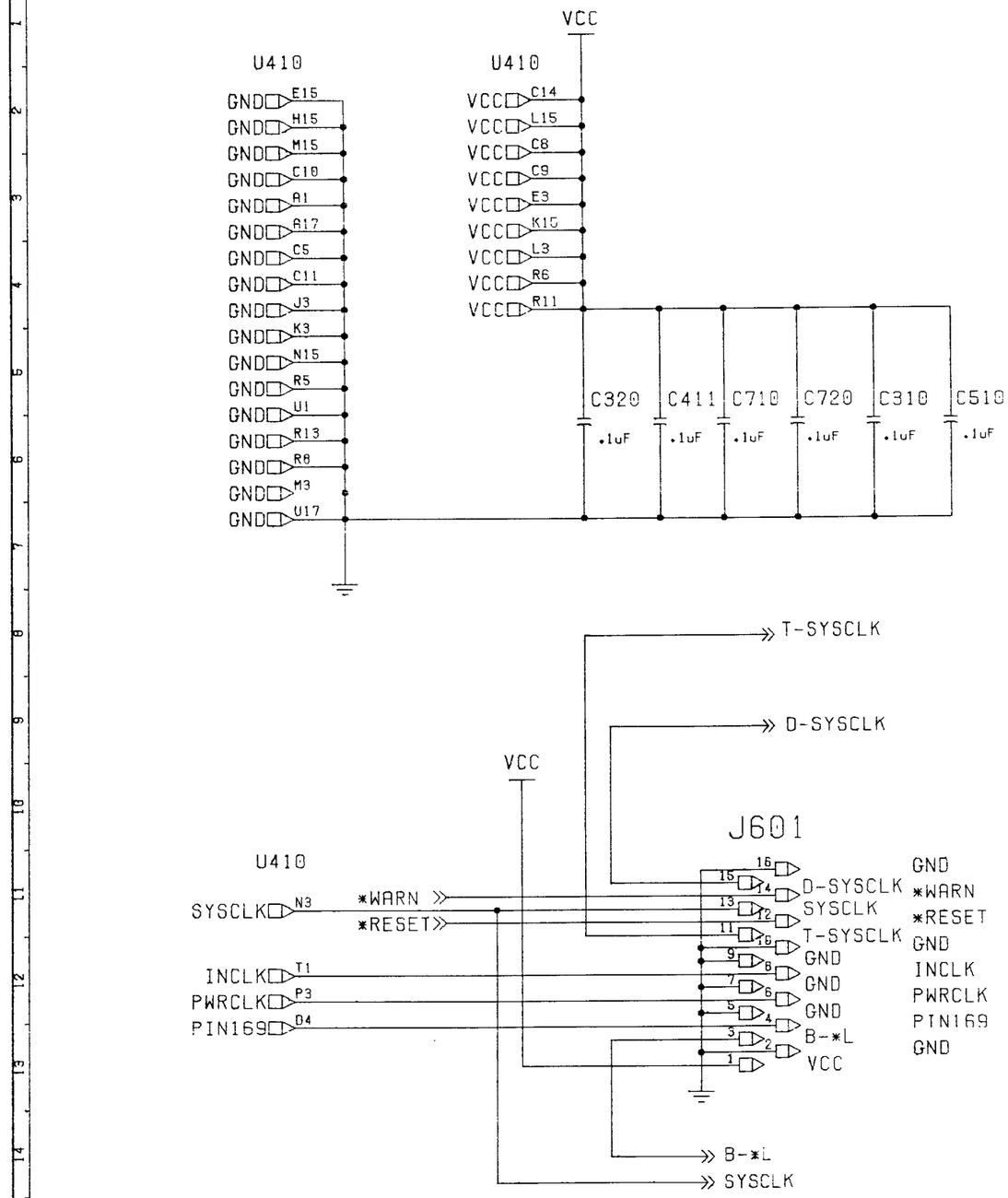

NOTES:	TEKTRONIX
	92DM72A Am29000/050
	PROBE ADAPTER
	SHEET 7 OF 7 REV 1

Replaceable Mechanical Parts

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

ITEM NAME

In the Parts List, an item Name is separated from the description by a colon(:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

1 2 3 4 5 Name & Description

Assembly and/or Component
Attaching parts for Assembly and/or Component

END ATTACHING PARTS

Detail Part of Assembly and/or Component
Attaching parts for Detail Part

END ATTACHING PARTS

Parts of Detail Part
Attaching parts for Parts of Detail Part

END ATTACHING PARTS

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation.

Attaching parts must be purchased separately, unless otherwise specified.

ABBREVIATIONS

Abbreviations conform to American National Standards Institute Y1.1

CROSS INDEX – MFR CODE NUMBER TO MANUFACTURER

Mfr Code	Manufacturer	Address	City, State, Zip Code
22526	DU PONT E I DE NEMOURS AND CO INC	515 FISHING CREEK RD	NEW CUMBERLAND PA 17070-3007
53387	MINNESOTA MINING MFG CO	PO BOX 2963	AUSTIN TX 78769-2963
63058	MCKENZIE TECHNOLOGY	44370 OLD WARMS SPRINGS BLVD	FREMONT CA 94538
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR	BEAVERTON OR 97077-0001
TK1462	YAMAICHI ELECTRONICS CO LTD	3-CHROME SHIBAURA	TOKYO JAPAN
	2ND FLOOR NEW KYOEI	MINATO-KU	

REPLACEABLE MECHANICAL PARTS

Fig. & Index No.	Tektronix Part Number	Serial Number Effect	Serial Number Discont	Qty	12345 Part Name & Description	Mfr Code	Mfr Part Number
C-6	010-0515-00			1	ADAPTER,PROBE:92DM72,29000 PGA 169 SOCKETED	80009	010-0515-00
-1	136-1144-00			1	.SKT,PL-IN ELEK:PGA,ZIF;17 X 17,169 PIN	TK1462	NP35-28916-G42AF-169
-2	671-1977-00			1	.CIRCUIT BD ASSY:92DM72 29000 PROBE ADAPTER	80009	671-1977-00
-3	----- -----			1	..SKT,PL-IN ELEK:PGA,169 PIN,17 X 17,LONG P (NOT REPLACEABLE,ORDER 671-1977-XX)		
-4	131-5267-00			8	..TERMINAL PIN:0.345 L X 0.100,0.025 SQ,GOL	53387	DHY-2072-001A10-57E
-5	131-3199-00			2	..BUS,CONDUCTOR:SHUNT,1 X 2,0.1 CTR,JUMPER	22526	68786-202
-6	136-1142-00			2	.SKT,PL-IN ELEK:PGA,169 PIN,17 X 17,SHORT	63058	PGA169H101B11709F
					STANDARD ACCESSORY		
	070-8477-00			1	MANUAL,TECH:INSTRUCTION,92DM72A 29000	80009	070-8477-00

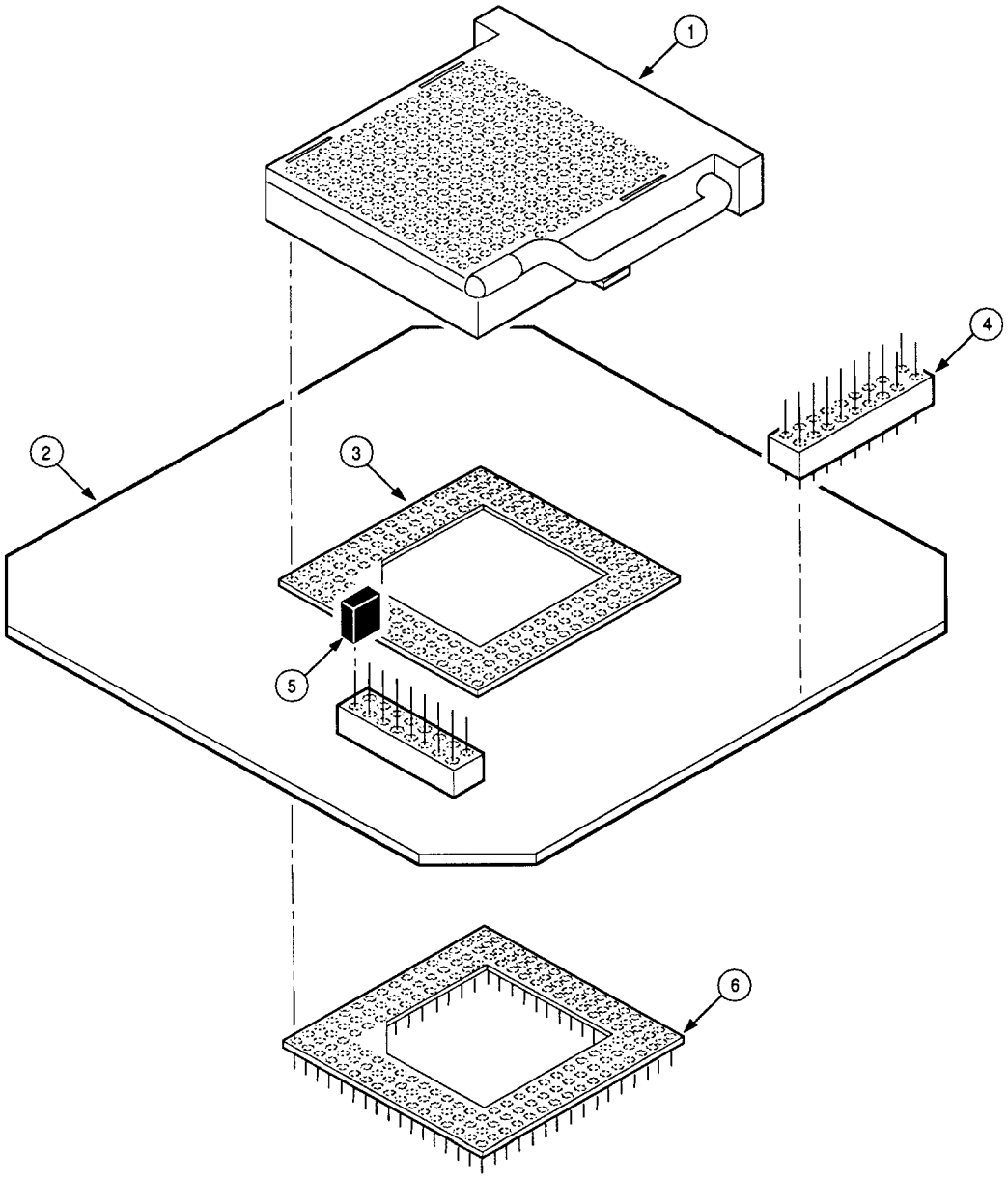

Figure C-6. Probe adapter exploded view.

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